

TPV-INVENTA TECHNOLOGY CO.,LTD.(TNI)

RDC2. EE Div. HW Department II

Board name : MotherBoard Schematic

Project : Nell (Nisene2 LarryBird)

Version : M0E

Initial Date : 2012/08/17

PCB P/N. : 6050A2516301

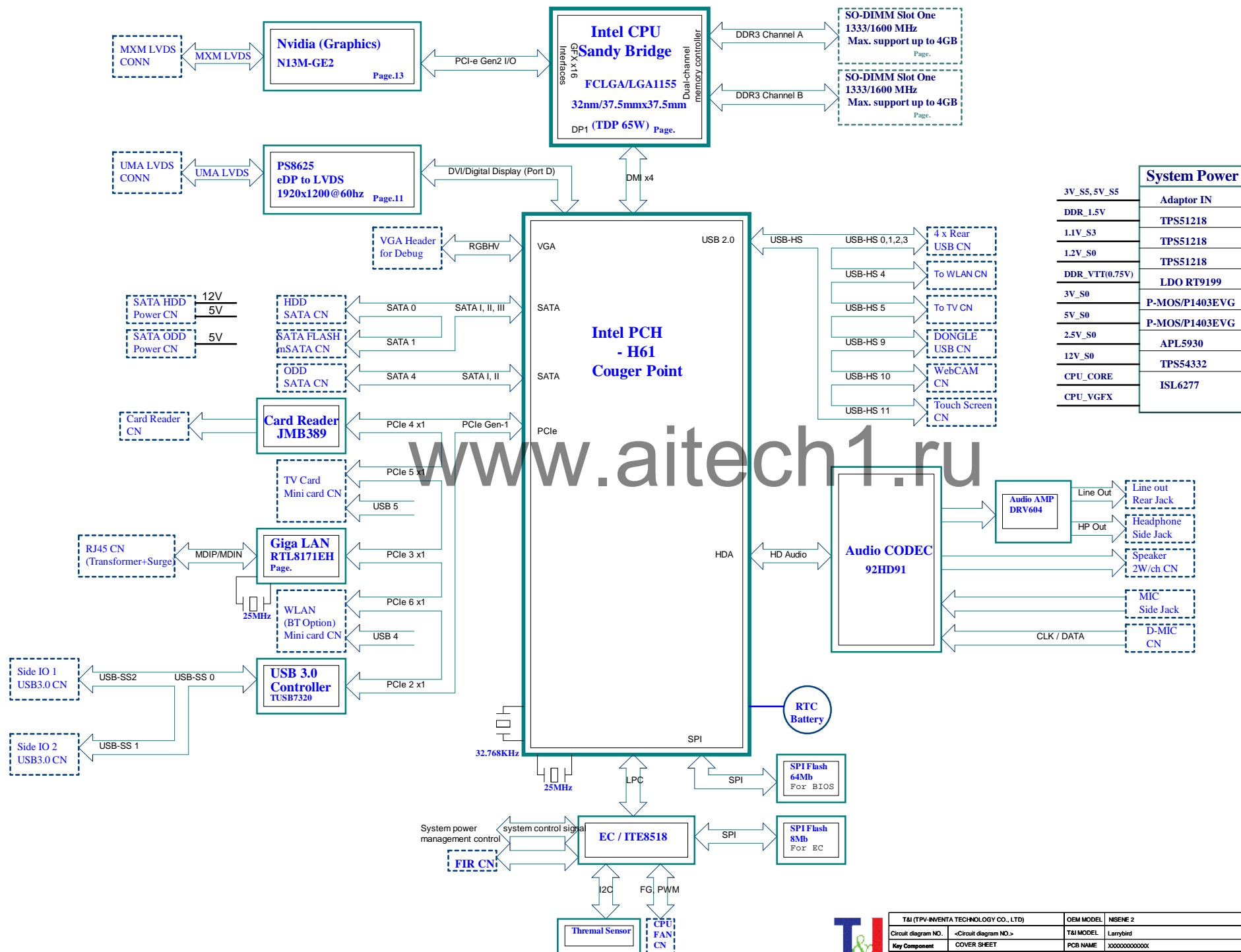
PCBA P/N. : 1310A2516301

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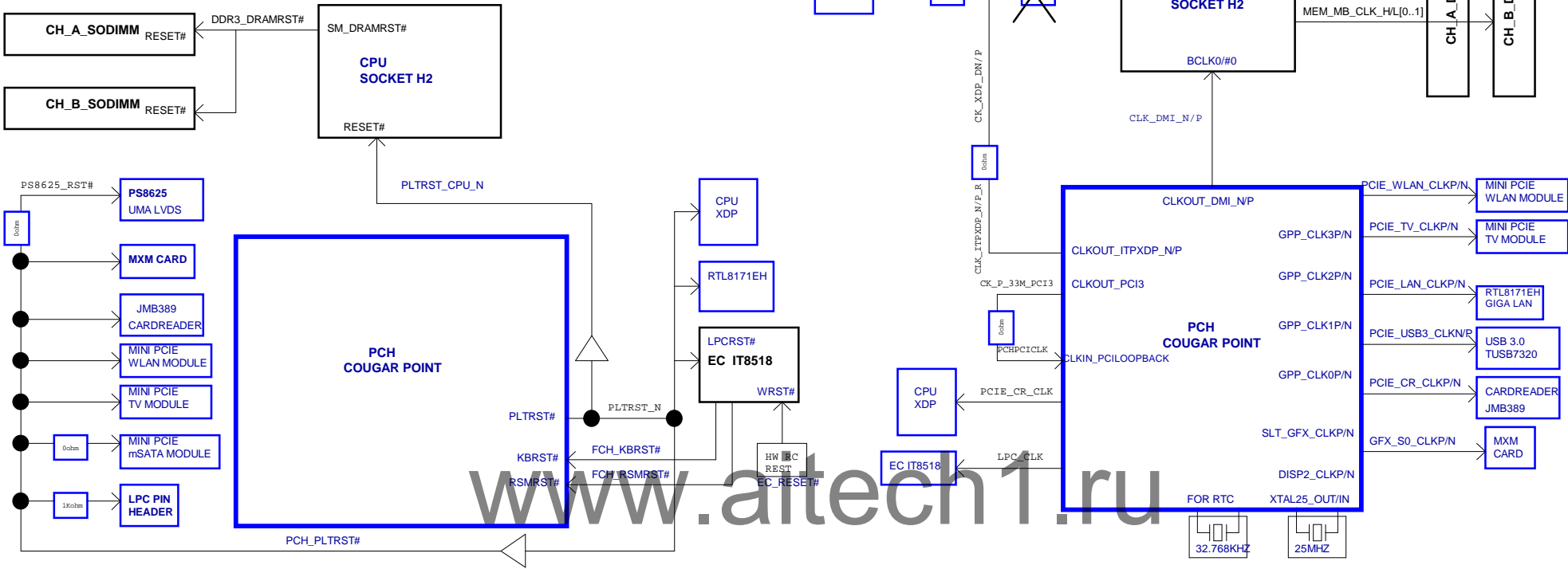
TNI (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	M0E
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	1 of 41		

03 SYSTEM BLOCK DIAGRAM

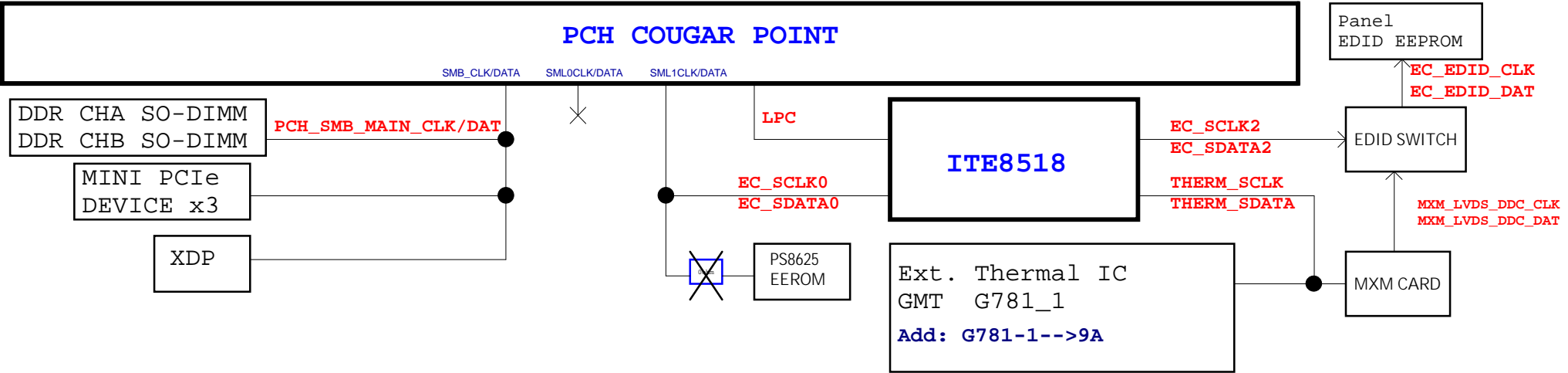


T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MOE
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	3 of 41		

RESET Block Diagram

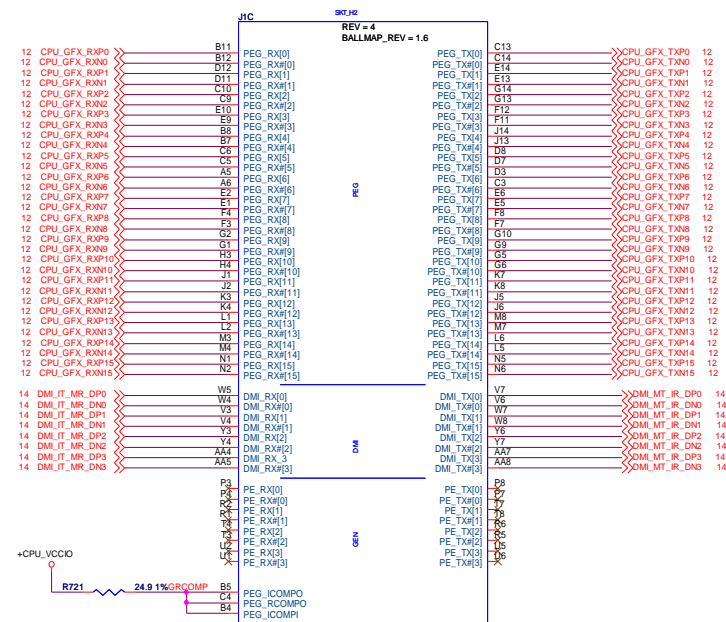


SM Bus MAP



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	M0E
Key Component	COVER SHEET	PCB NAME	J000000000000	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	4 of 41		

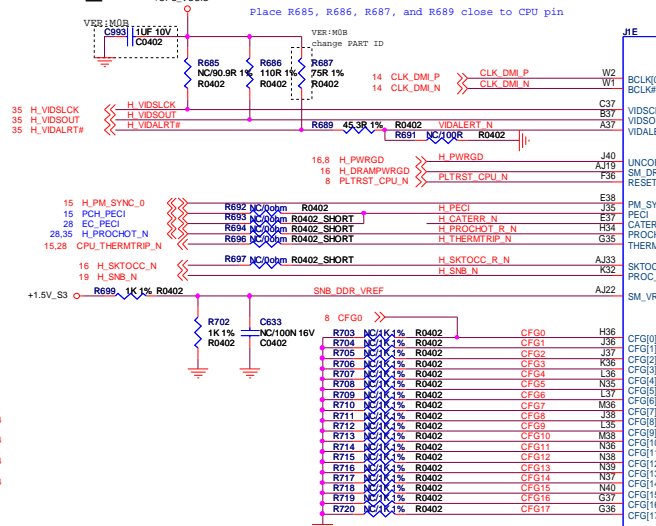
PCIEX16 & DMI



Note:

- (1).SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R81
- (2).ROUTE B5 TO R81 AS A SEPERATE 12 MIL TRACE
- (3).PCIE X4 LANES ARE NOT SUPPORTED ON DESKTOP CPU SKUS

H2_E

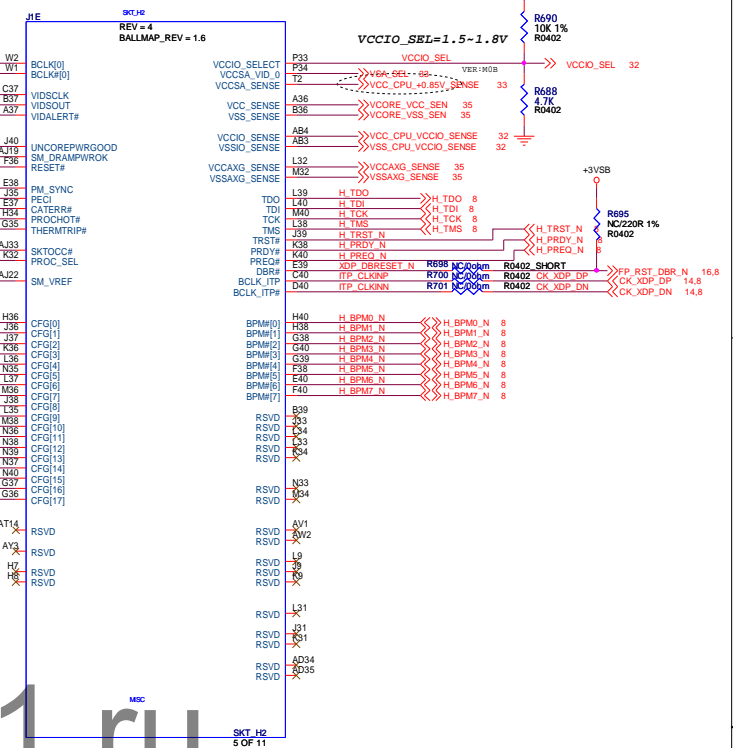


Below configuration is defined on CRB page 14.

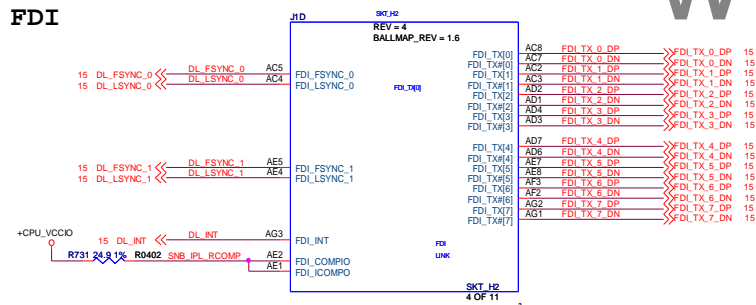
```
CFG2-->H-->NORM-->L-->REVERSE
CFG5-->SEL(0)-->H
CFG6-->SEL(1)-->H
1X16

CFG5-->SEL(0)-->L
CFG6-->SEL(1)-->H
2X8

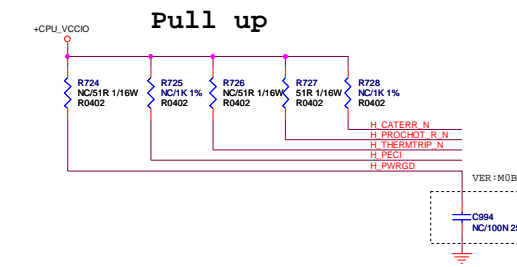
CFG5-->SEL(0)-->L
CFG6-->SEL(1)-->L
```



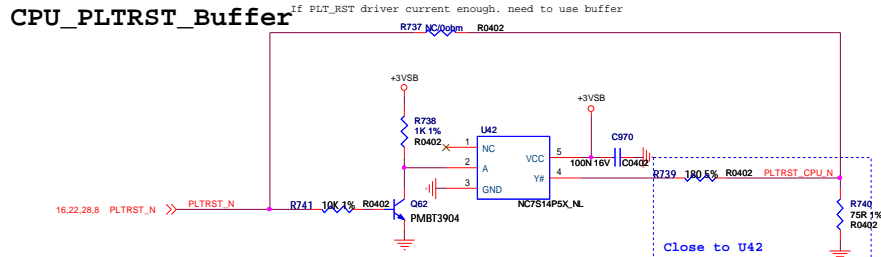
FDI



Pull up

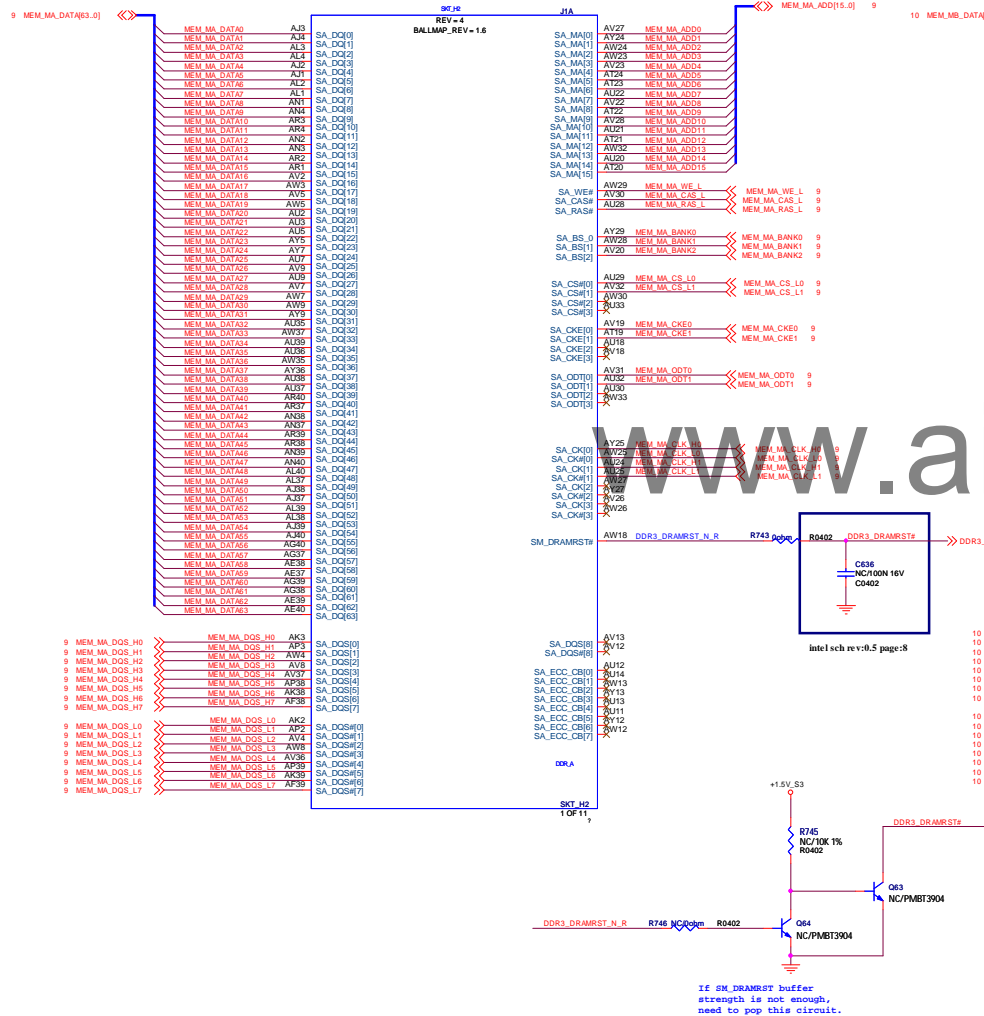
CPU PLTRST Buffer¹

If PLT_RST driver current enough. need to use buffer

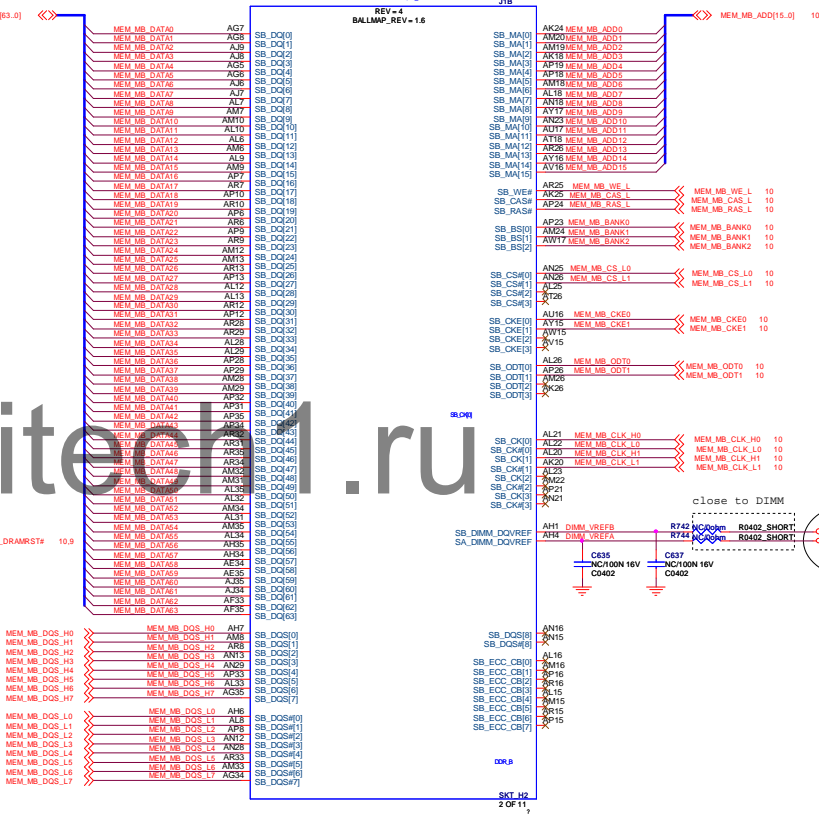


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Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXXXX	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	5 of 41		

Channel_A

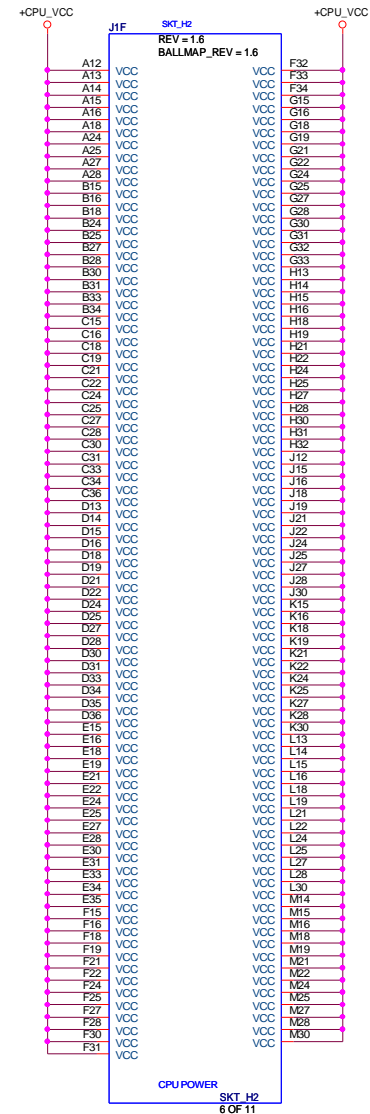


Channel_B

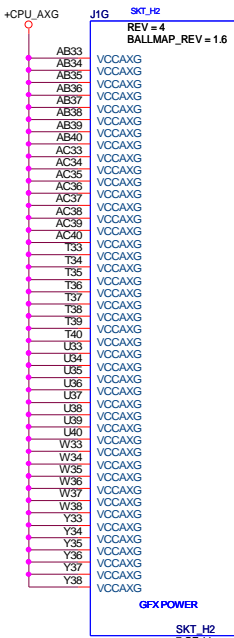


If SM_DRAMRST buffer strength is not enough, need to pop this circuit.

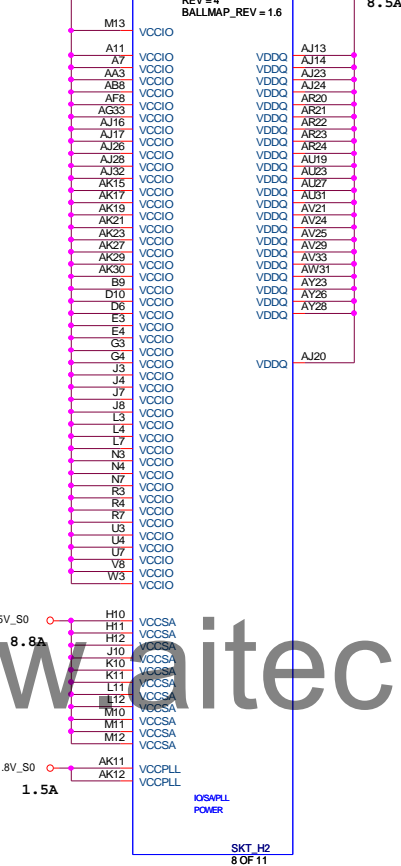
75A



35A

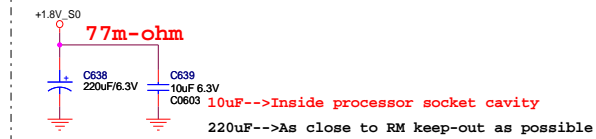


8.5A

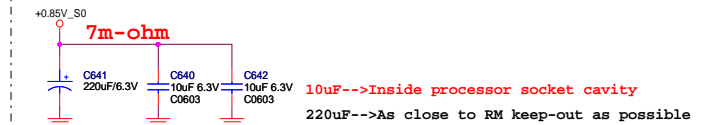


+1.5V_S3

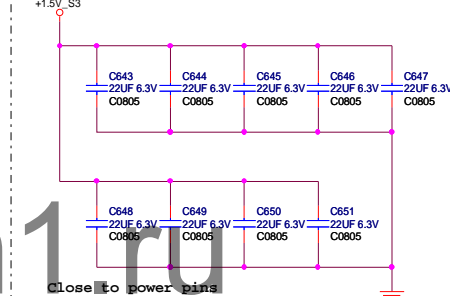
+1.8V_S0-->Decoupling



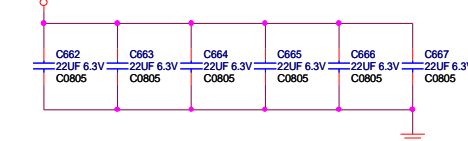
+0.85V_S0-->Decoupling



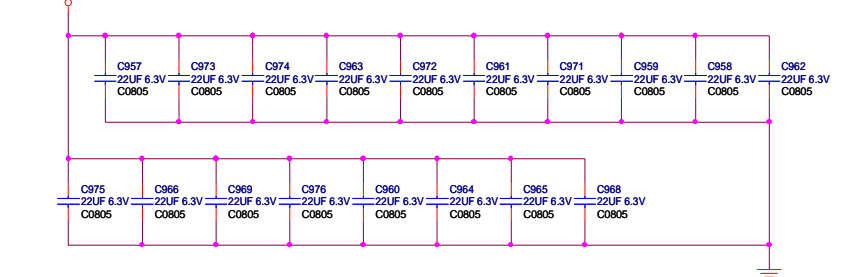
+1.5V_S0-->Decoupling



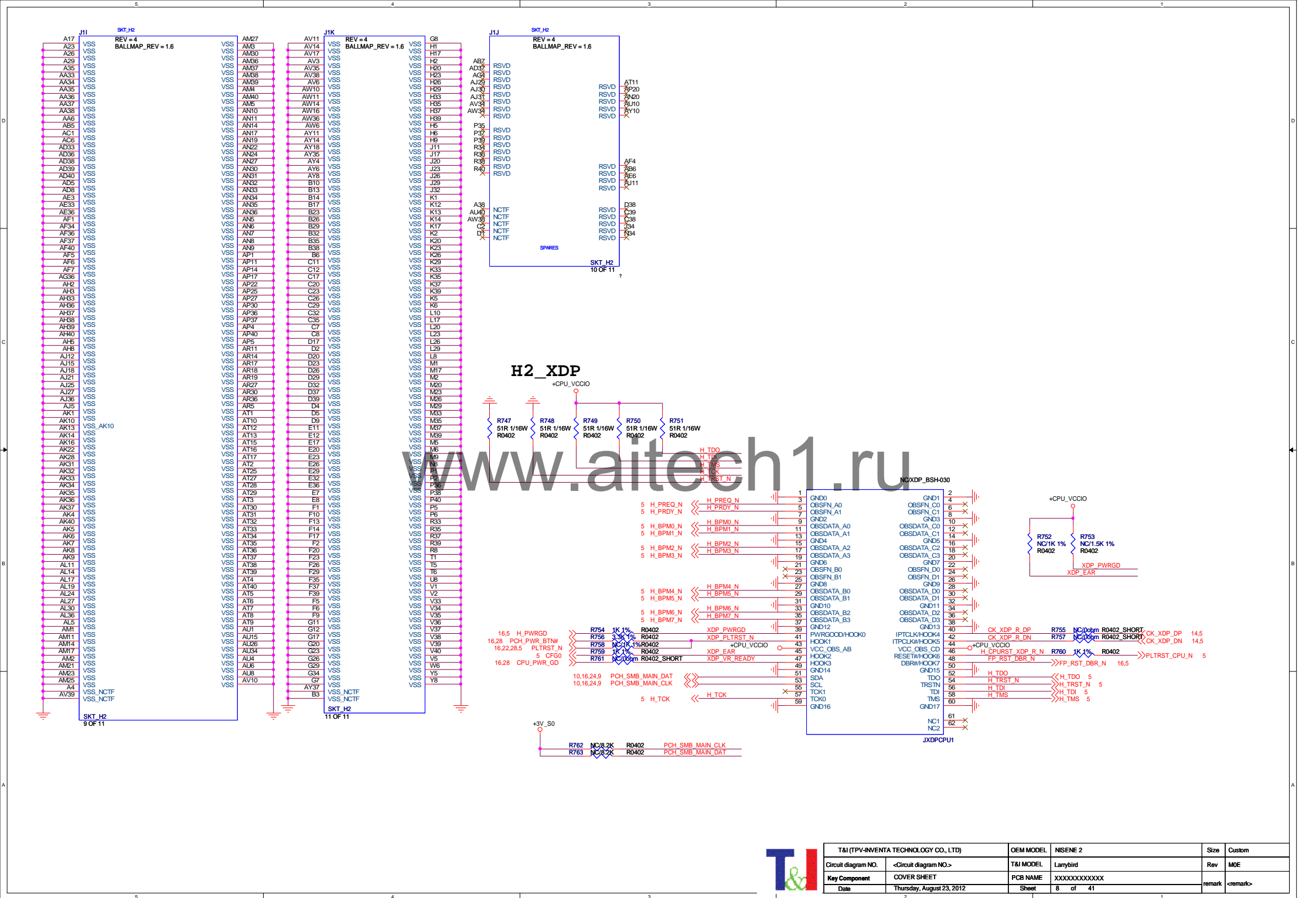
+CPU_AXG



+CPU_VCCIO

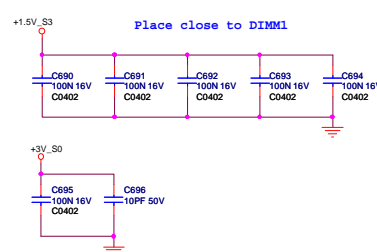
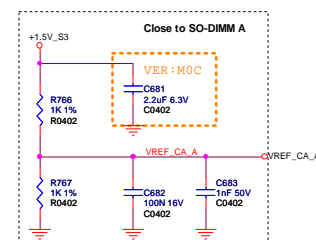
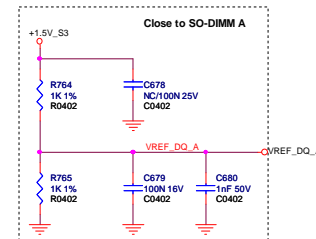



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, August 23, 2012	Sheet	7 of 41	<remark>



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	Custom
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, August 23, 2012	Sheet	8 of 41	<remark>

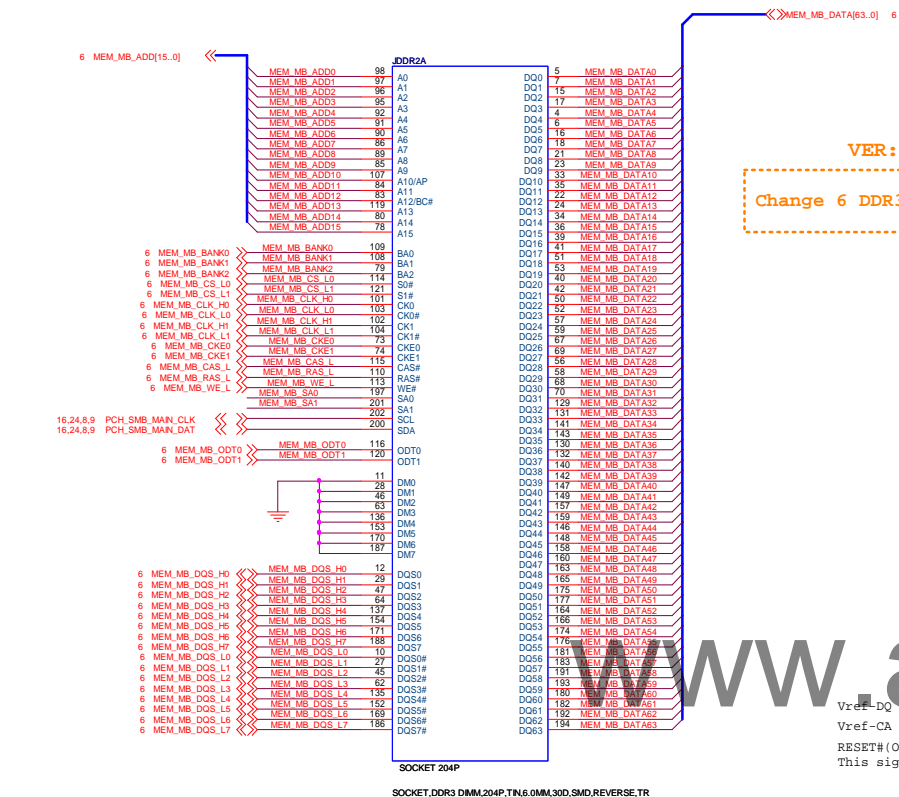
CHA DDR 10.1H(DIMM-1)



	T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NSENE 2	Size	C
	Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MOE
	Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXXXXXXXX	remark	<remark>
	Date	Thursday, August 23, 2012	Sheet	9 of 41		

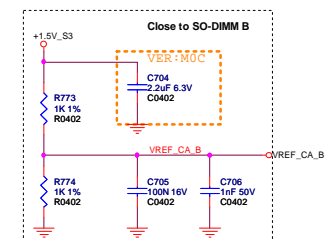
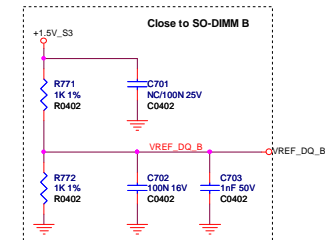
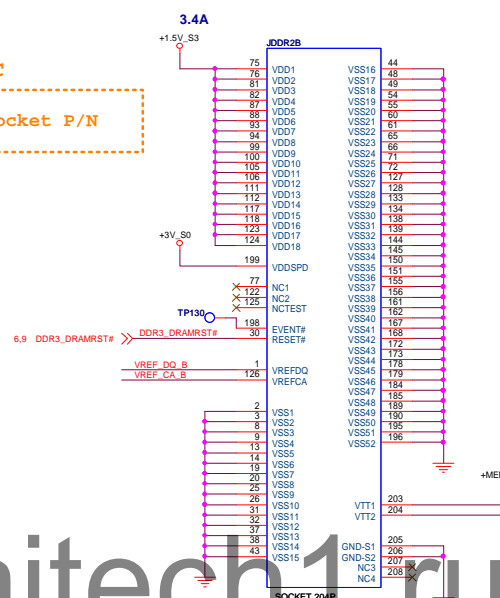
VER:M0B
JDDR1 is change to 6.0mm height

CHB DDR 6.0H(DIMM-2)

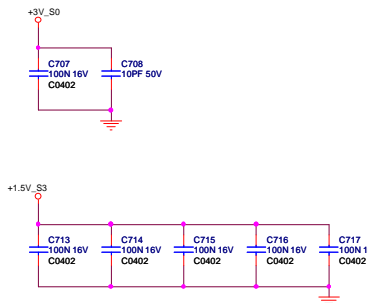
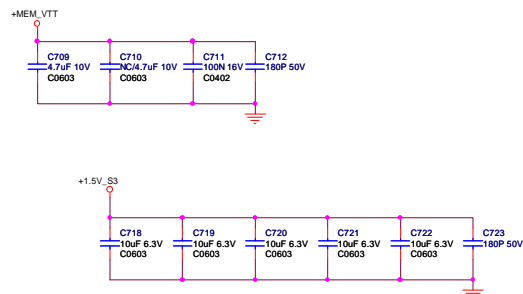
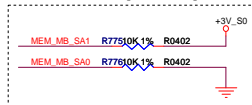


VER:M0C

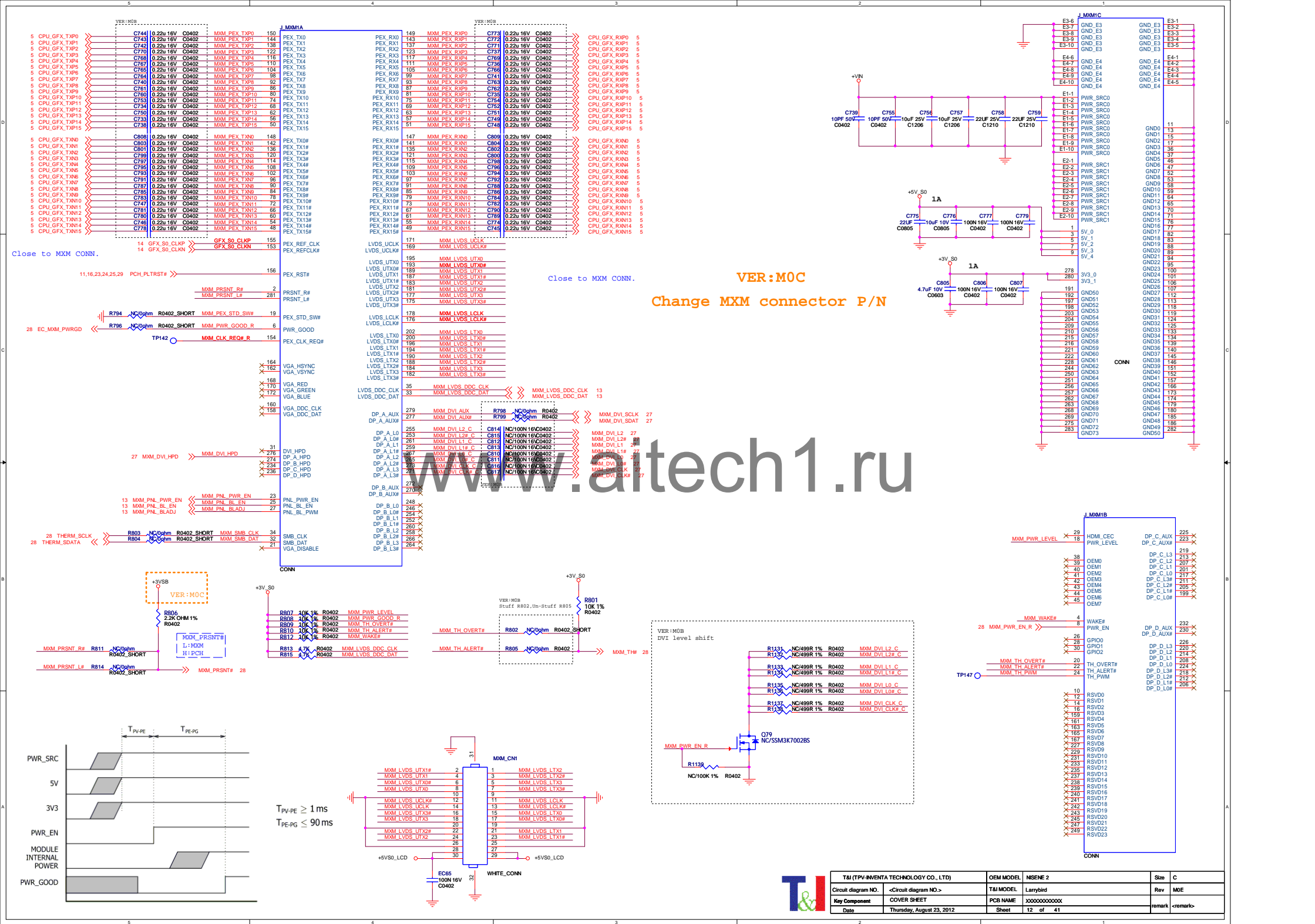
Change 6 DDR3 Socket P/N



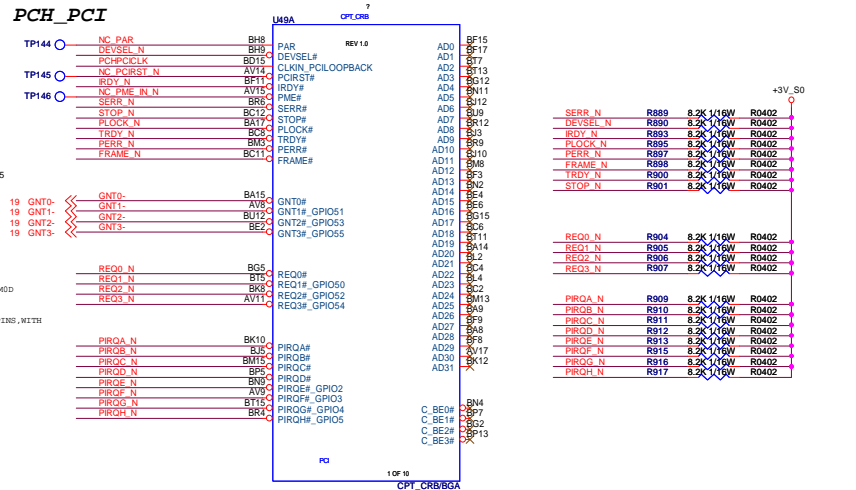
DIMM2 (CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	J000000000000	remark
Date	Thursday, August 23, 2012	Sheet	10 of 41	<remark>



PCH PCI



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2		Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird		Rev	MDE
Key Component	COVER SHEET	PCS NAME	X00000000000X		remark	<remark>
Date	Thursday, August 23, 2012	Sheet	14 of 41			

PCH_SATA

PCH_MEPWR0K:
1).V_1P05_ME
2).PCH_SLP_A

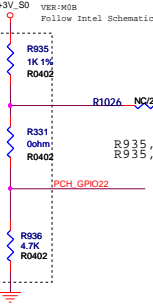
Not available in Mobile & Desktop

VER:M0C

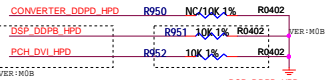
VER:M0C

PCH_CONFIG Recovery

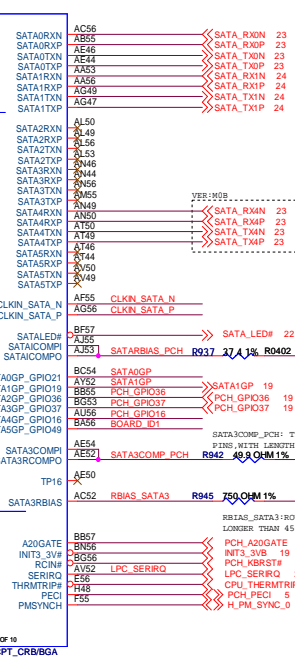
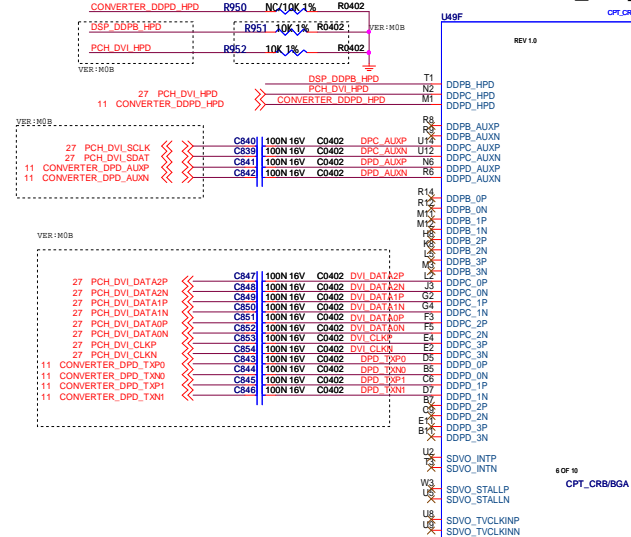
R935, R331, R936 -- Normal (Default)
R935, R1026 -- CONFIGURE



No VGA (pull down)



PCH_Display



3.5" HDD

mSATA

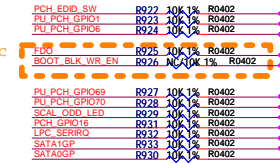
ODD

SATA3COMP_PCH: TIE TRACES TOGETHER CLOSE TO PINS WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

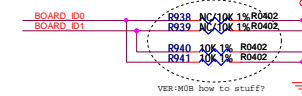
BIAS_SATA3/ROUTER TRACE LENGTH NO LONGER THAN 450 MILS TO RESISTOR

PCH_A20GATE 28
INT3_3V8 19
PCH_KBRST# 28
LPC_SERRQ 28.29
CPL_THERMTRIP_N 28.5
PCH_PECI 5
H_P.M_SYNC_0 5

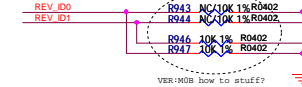
Pull HIGH for PCH



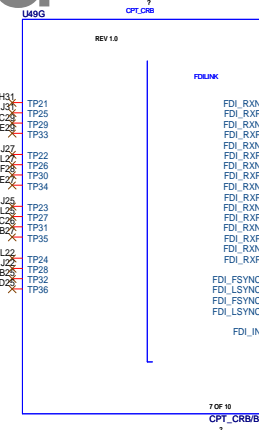
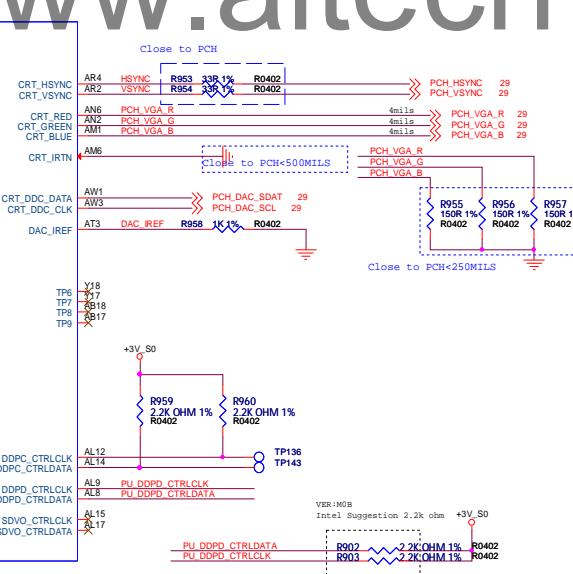
BOARD ID



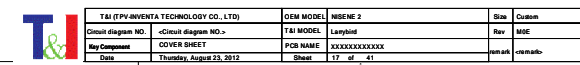
REV ID

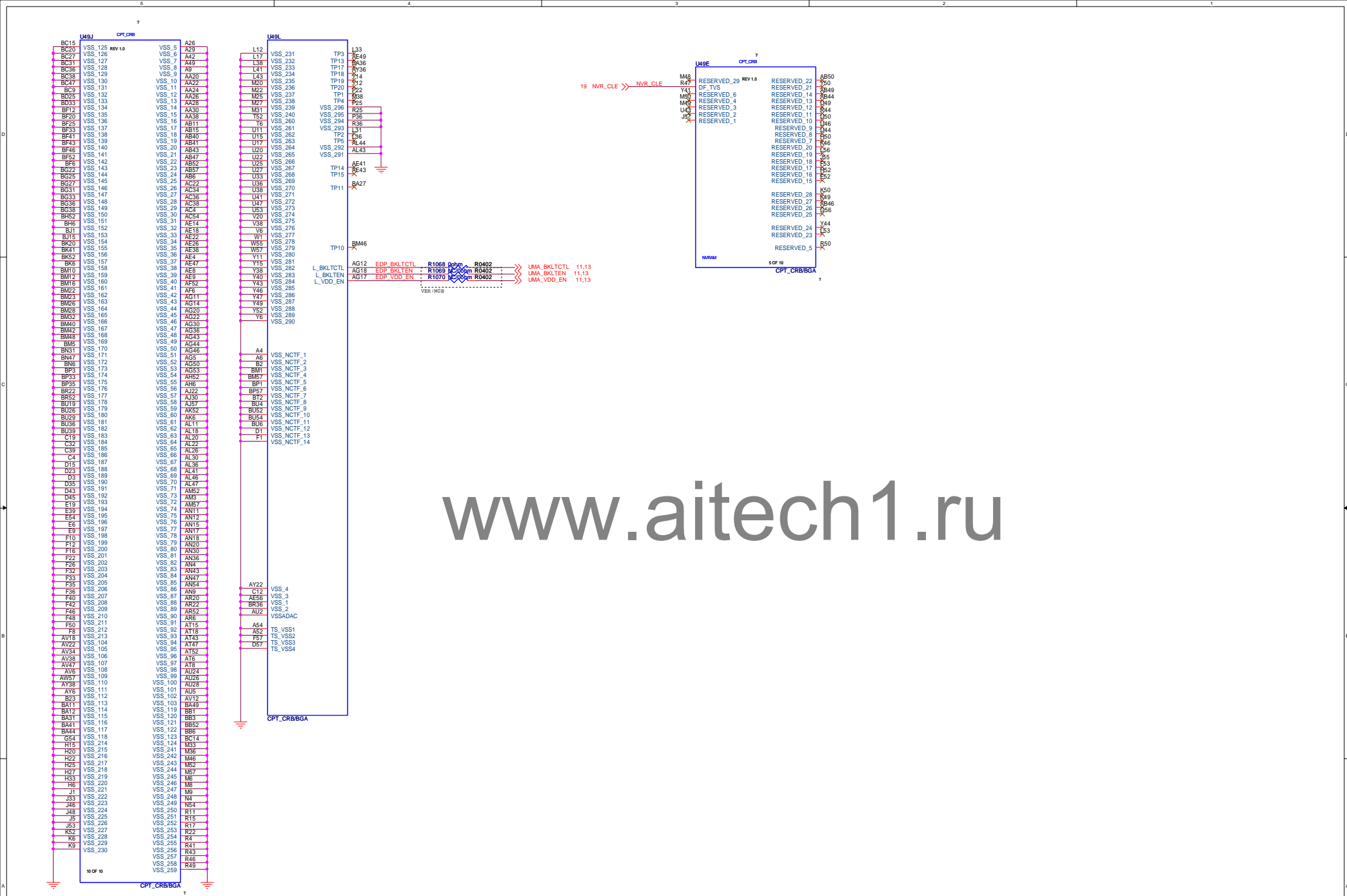


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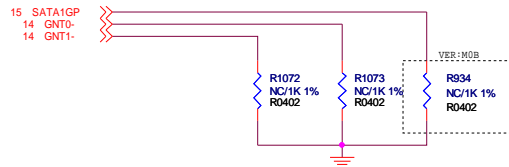
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXX	remark
Date	Thursday, August 23, 2012	Sheet	15 of 41	<remark>





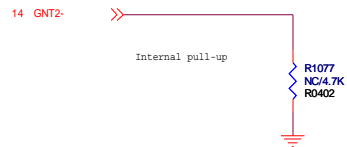
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	M0E
Key Component	COVER SHEET	PCB NAME	X0000000000X	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	18 of 41		

CP REQUIRED STRAPS

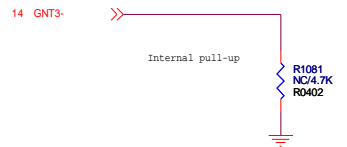


BOOT select straps

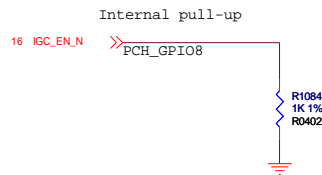
GNT1-	SATA1GP	Boot device
0	0	LPC
1	0	PCI
1	1	SPI(Default)



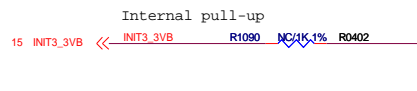
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up

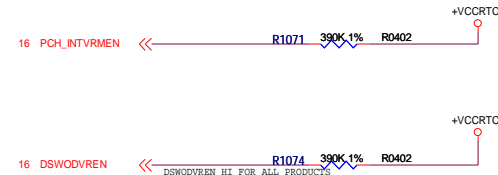


GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

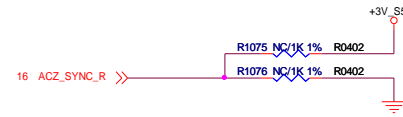


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the
integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

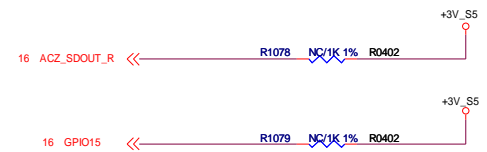
This signal enables the internal Deep Sleep 1.05 V
regulators. Must be connected even when not supporting DSW.



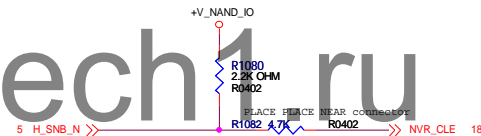
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

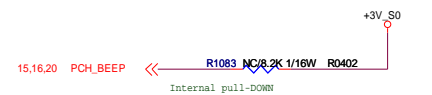
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



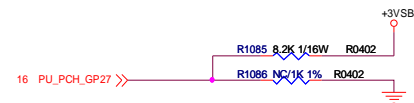
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



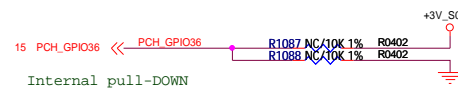
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



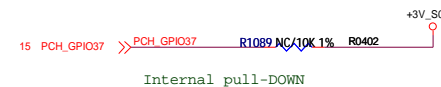
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



In Deep Sleep Power Well.
If not used, require a weak pull-up(8.2k-10k) to VccDSW3_3



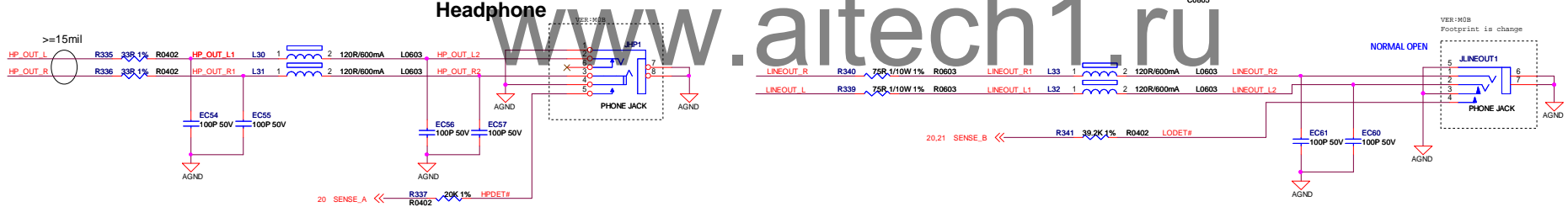
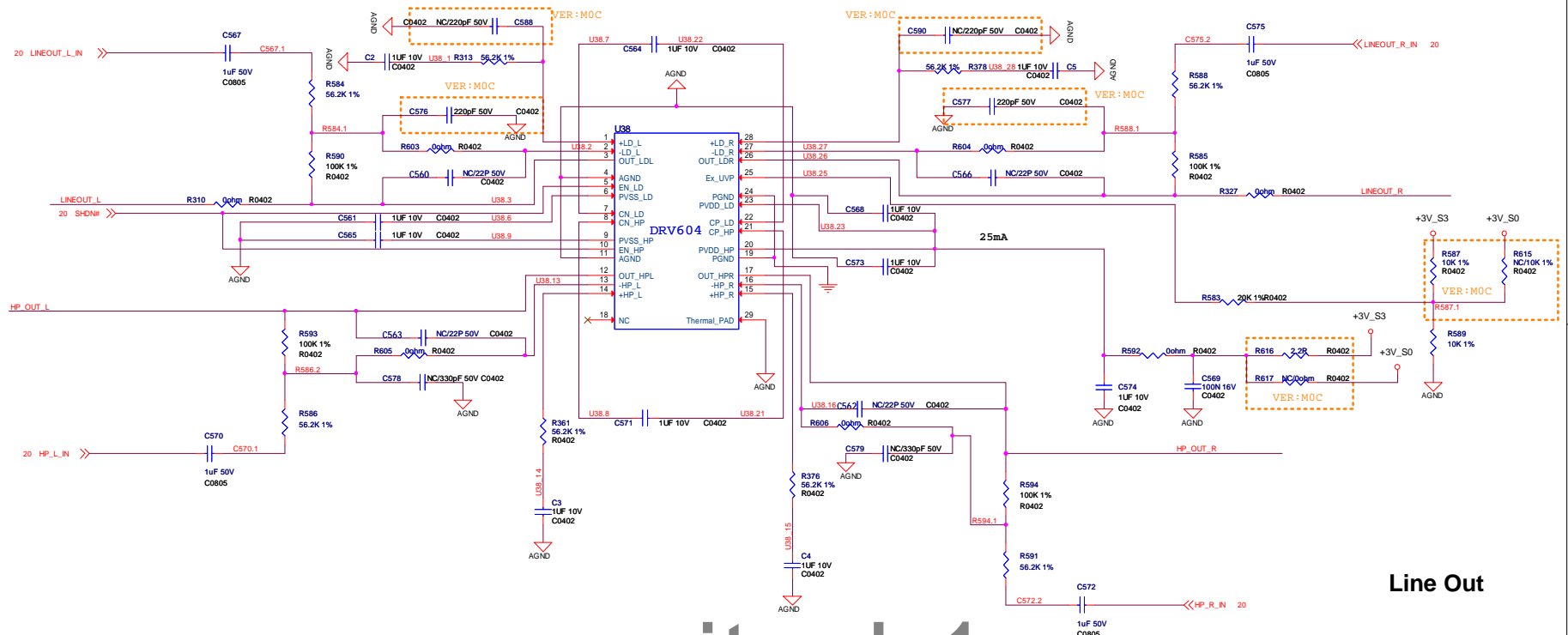
Cougar point EDS PAGE:93 This signal should not be pull high



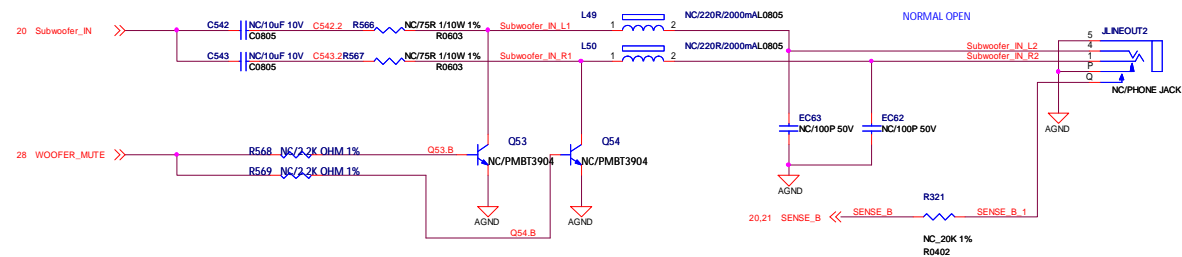
Cougar point EDS PAGE:93 This signal should not be pull high



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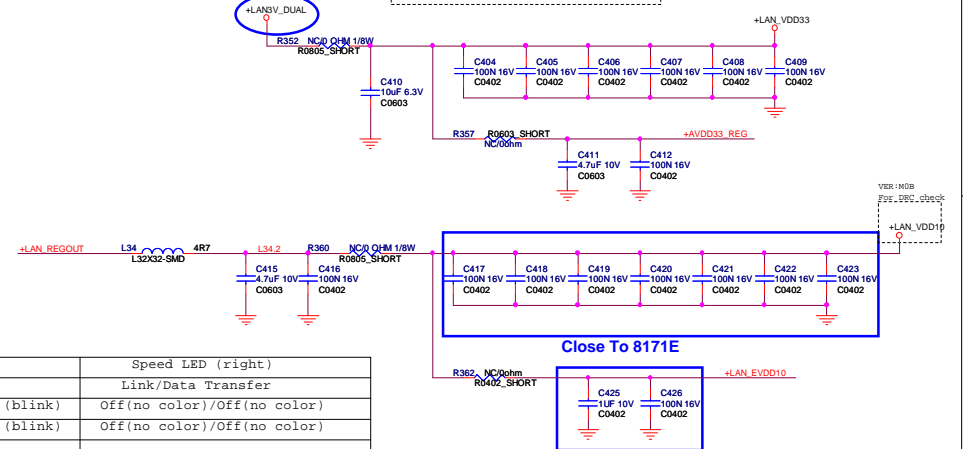
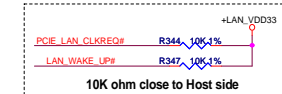
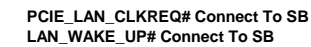
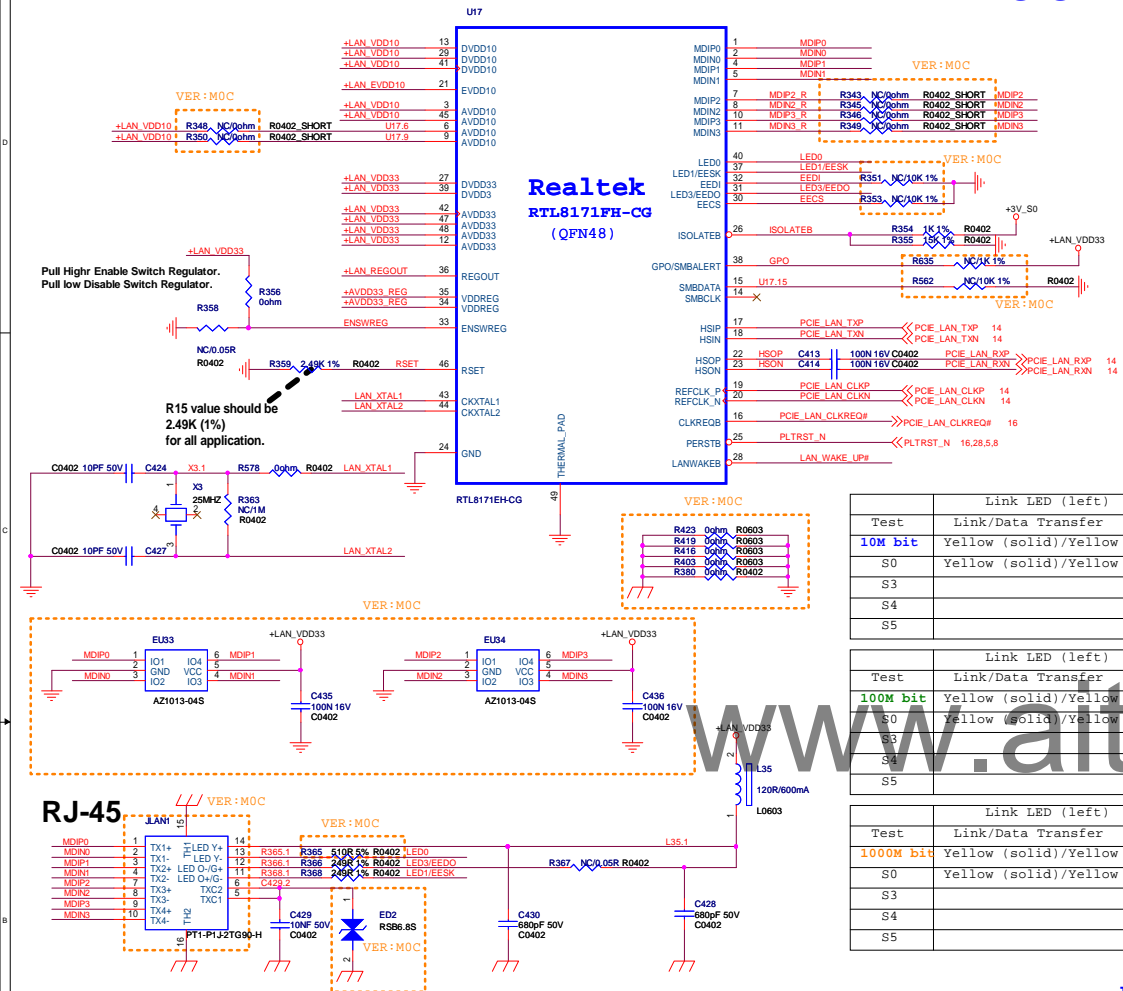


Subwoofer



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	X0000000000X	MOE
Date	Thursday, August 23, 2012	Sheet	21 of 41	remark
				<remark>

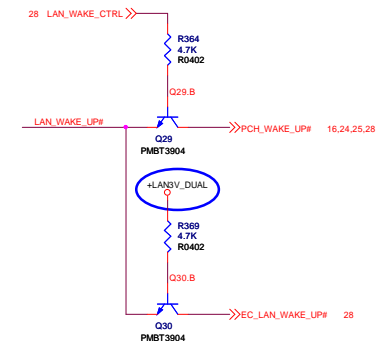
GIGA LAN



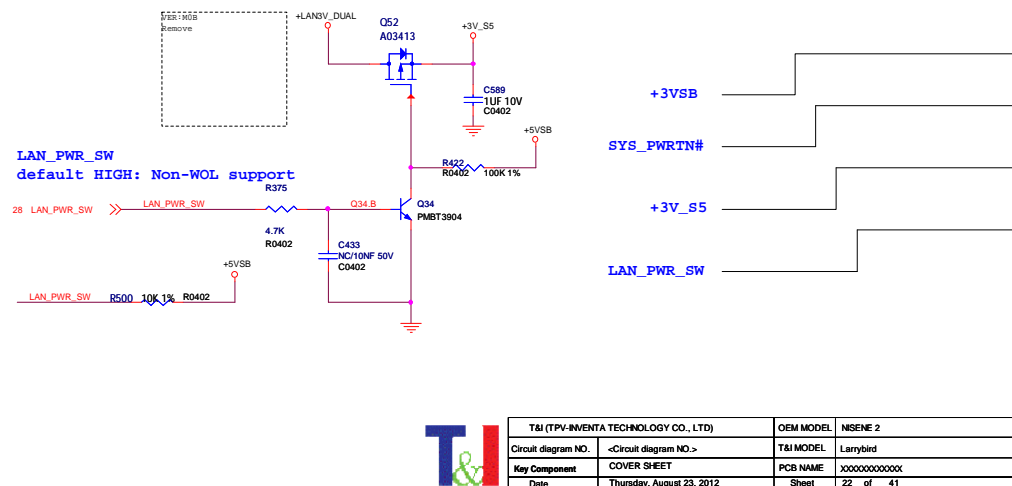
	Link LED (left)	Speed LED (right)
Test	Link/Data Transfer	Link/Data Transfer
10M bit	Yellow (solid)/Yellow (blink)	Off(no color)/Off(no color)
S0	Yellow (solid)/Yellow (blink)	Off(no color)/Off(no color)
S3		
S4		
S5		

	Link LED (left)	Speed LED (right)
Test	Link/Data Transfer	Link/Data Transfer
100M bit	Yellow (solid)/Yellow (blink)	Orange (solid)/Orange (solid)
S0	Yellow (solid)/Yellow (blink)	Orange (solid)/Orange (solid)
S3		
S4		
S5		

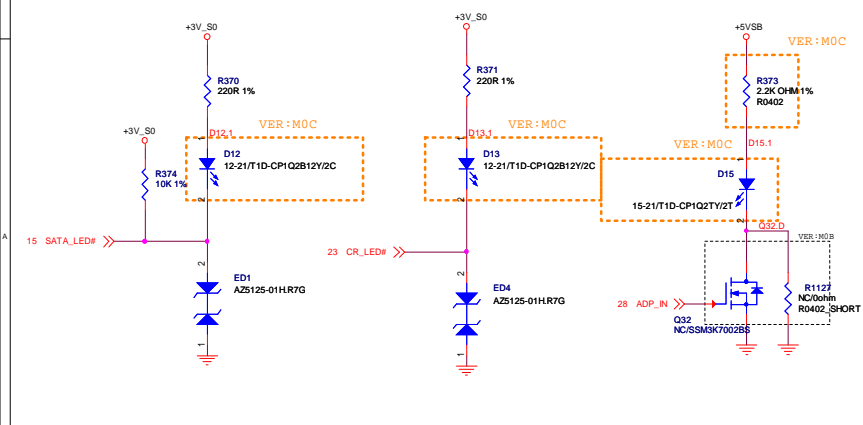
	Link LED (left)	Speed LED (right)
Test	Link/Data Transfer	Link/Data Transfer
1000M b/s	Yellow (solid)/Yellow (blink)	Green (solid)/Green (solid)
S0	Yellow (solid)/Yellow (blink)	Green (solid)/Green (solid)
S3		
S4		
S5		



LAN POWER SWITCH

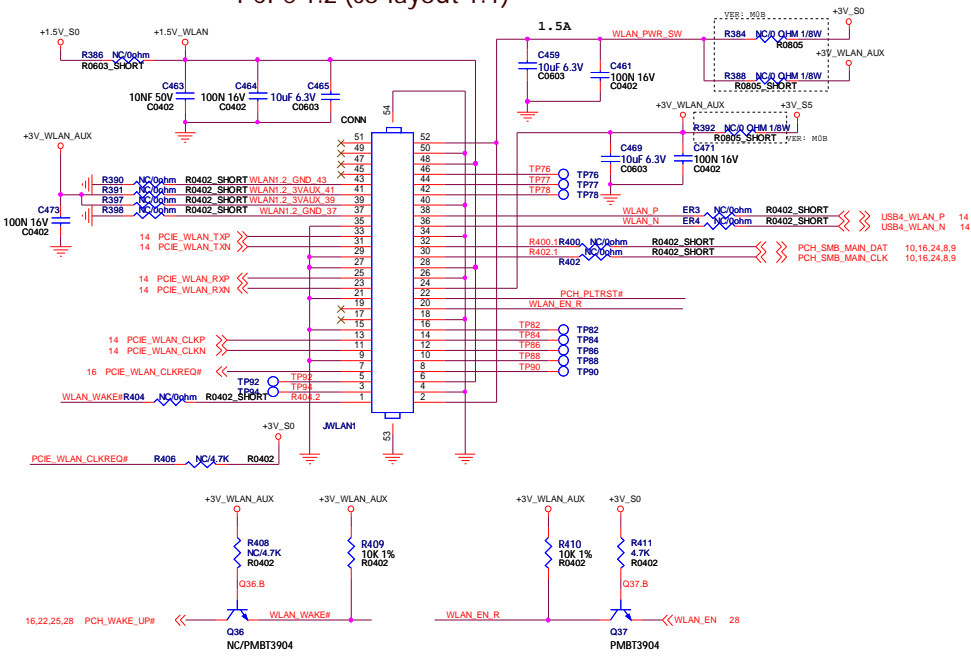


LED



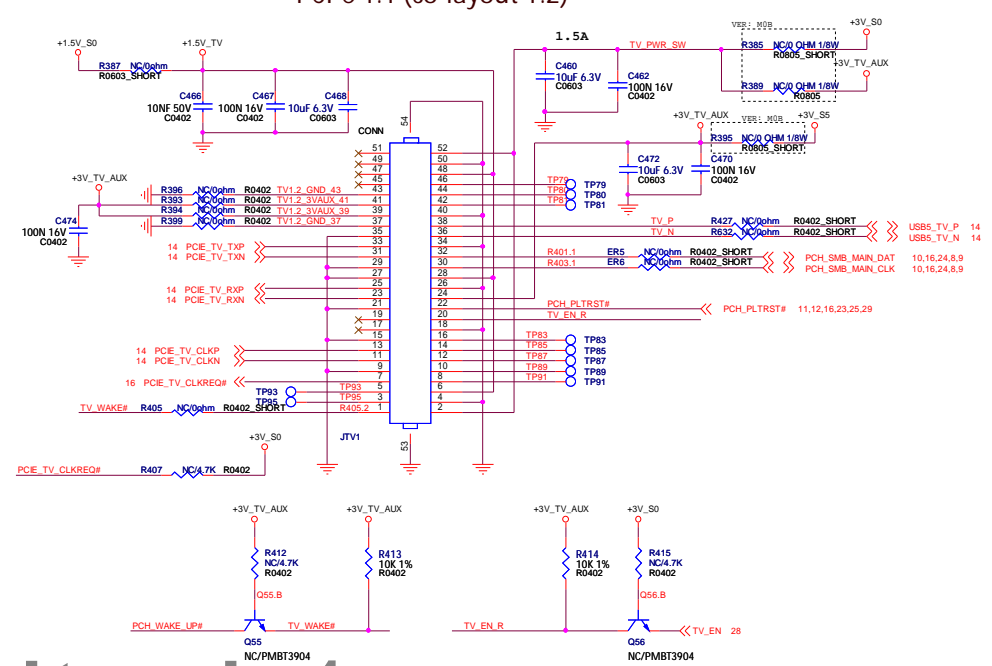
MINI PCI-E WLAN & BT

PCI-e 1.2 (co-layout 1.1)



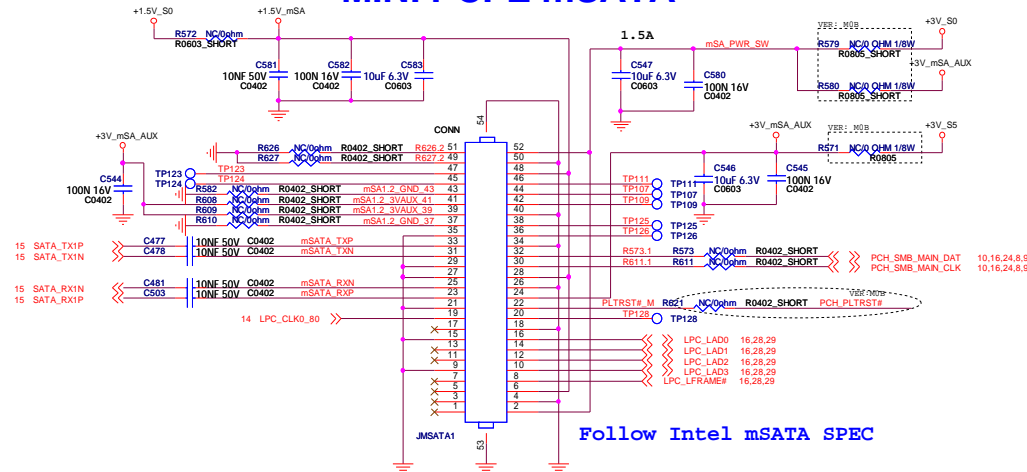
MINI PCI-E TV CARD

PCI-e 1.1 (co-layout 1.2)

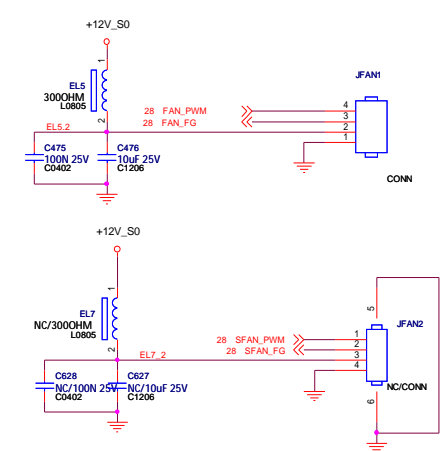


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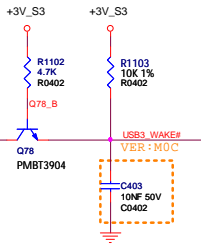
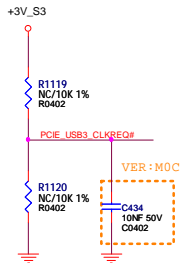
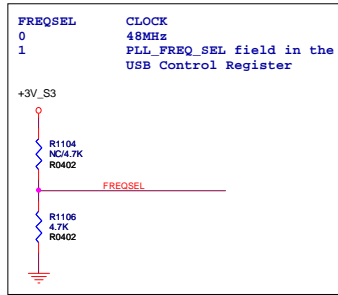
MINI PCI-E mSATA



CPU Linear FAN Control



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	Larrybird	Rev	M0E
Key Component	COVER SHEET	PCB NAME	J000000000000	remark
Date	Thursday, August 23, 2012	Sheet	24 of 41	<remark>



POPULATE PULLDOWN IF I2C EEPROM
NOT USED AND DO NOT POPULATE
PULLUP.

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PLACE CLOSE TO U1

R1105 0.0K 1% R0402

R1EXT

R1EXTRTN

FREQSEL

VSS_OSC

USB3_X0

USB3_X1

VER:M0B

Change to 18pF

C921 18PF 50V J C0402

C922 18PF 50V C0402

X6

48MHz

R1107 1M R0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

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C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

C403 10NF 50V C0402

VER:M0C

R1091 FOR WAKE SUPPORT

R1091 10K 1% R0402

R1092 FOR NO WAKE SUPPORT

R1092 NC/10K 1% R0402

R1093 NC/10K 1% R0402

R1094 NC/2.2K 0.1M R0402

R1095 NC/2.2K 0.1M R0402

R1096 NC/10K 1% R0402

R1097 NC/10K 1% R0402

R1099 NC/10K 1% R0402

R1100 NC/10K 1% R0402

R1101 0.1M R0402

R1108 0.1M R0402

R1109 0.1M R0402

R1110 0.1M R0402

R1111 0.1M R0402

R1112 0.1M R0402

R1113 0.1M R0402

R1114 0.1M R0402

R1115 0.1M R0402

R1116 0.1M R0402

R1117 0.1M R0402

R1118 0.1M R0402

R1119 0.1M R0402

R1120 0.1M R0402

R1121 0.1M R0402

R1122 0.1M R0402

R1123 0.1M R0402

R1124 0.1M R0402

R1125 0.1M R0402

R1126 0.1M R0402

R1127 0.1M R0402

R1128 0.1M R0402

R1129 0.1M R0402

R1130 0.1M R0402

R1131 0.1M R0402

R1132 0.1M R0402

R1133 0.1M R0402

R1134 0.1M R0402

R1135 0.1M R0402

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R1170 0.1M R0402

R1171 0.1M R0402

R1172 0.1M R0402

R1173 0.1M R0402

R1174 0.1M R0402

R1175 0.1M R0402

R1176 0.1M R0402

R1177 0.1M R0402

R1178 0.1M R0402

R1179 0.1M R0402

R1180 0.1M R0402

R1181 0.1M R0402

R1182 0.1M R0402

R1183 0.1M R0402

R1184 0.1M R0402

R1185 0.1M R0402

R1186 0.1M R0402

R1187 0.1M R0402

R1188 0.1M R0402

R1189 0.1M R0402

R1190 0.1M R0402

R1191 0.1M R0402

R1192 0.1M R0402

R1193 0.1M R0402

R1194 0.1M R0402

R1195 0.1M R0402

R1196 0.1M R0402

R1197 0.1M R0402

R1198 0.1M R0402

R1199 0.1M R0402

R1200 0.1M R0402

R1201 0.1M R0402

R1202 0.1M R0402

R1203 0.1M R0402

R1204 0.1M R0402

R1205 0.1M R0402

R1206 0.1M R0402

R1207 0.1M R0402

R1208 0.1M R0402

R1209 0.1M R0402

R1210 0.1M R0402

R1211 0.1M R0402

R1212 0.1M R0402

R1213 0.1M R0402

R1214 0.1M R0402

R1215 0.1M R0402

R1216 0.1M R0402

R1217 0.1M R0402

R1218 0.1M R0402

R1219 0.1M R0402

R1220 0.1M R0402

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R1222 0.1M R0402

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R1224 0.1M R0402

R1225 0.1M R0402

R1226 0.1M R0402

R1227 0.1M R0402

R1228 0.1M R0402

R1229 0.1M R0402

R1230 0.1M R0402

R1231 0.1M R0402

R1232 0.1M R0402

R1233 0.1M R0402

R1234 0.1M R0402

R1235 0.1M R0402

R1236 0.1M R0402

R1237 0.1M R0402

R1238 0.1M R0402

R1239 0.1M R0402

R1240 0.1M R0402

R1241 0.1M R0402

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R1260 0.1M R0402

R1261 0.1M R0402

R1262 0.1M R0402

R1263 0.1M R0402

R1264 0.1M R0402

R1265 0.1M R0402

R1266 0.1M R0402

R1267 0.1M R0402

R1268 0.1M R0402

R1269 0.1M R0402

R1270 0.1M R0402

R1271 0.1M R0402

R1272 0.1M R0402

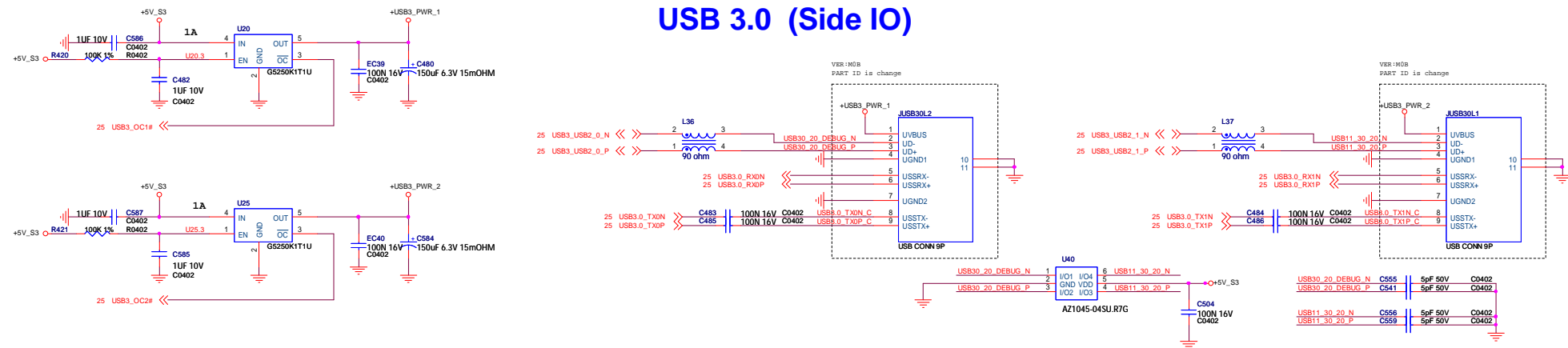
R1273 0.1M R0402

R1274 0.1M R0402

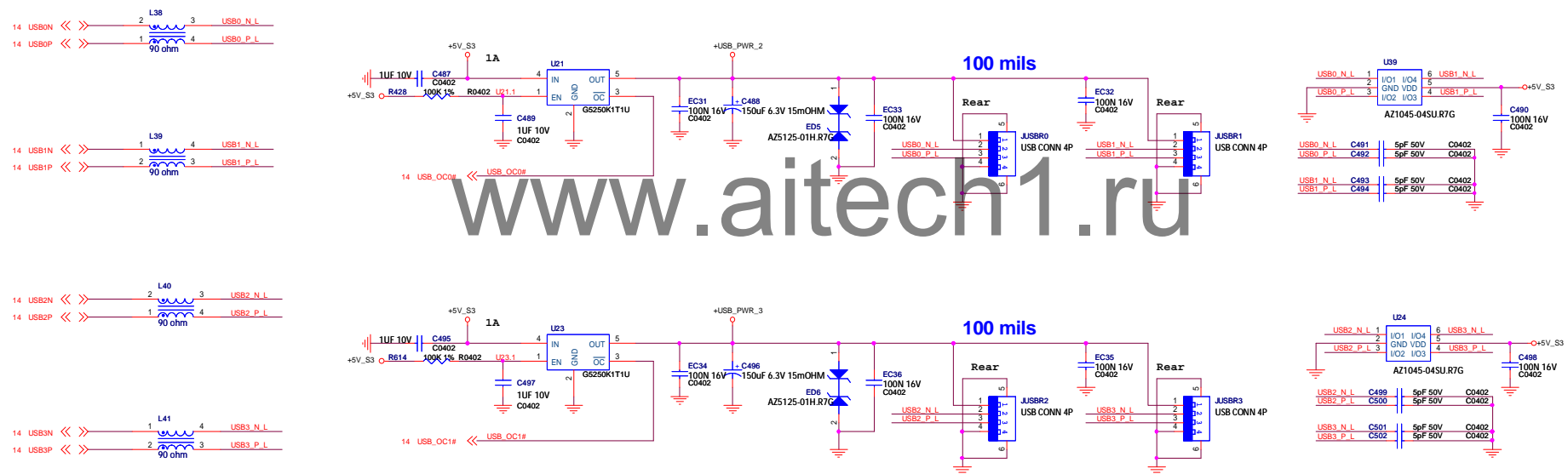
R1275 0.1M R0402

R1276 0.1M R0402

USB 3.0 (Side IO)



USB 2.0 (Rear IO)

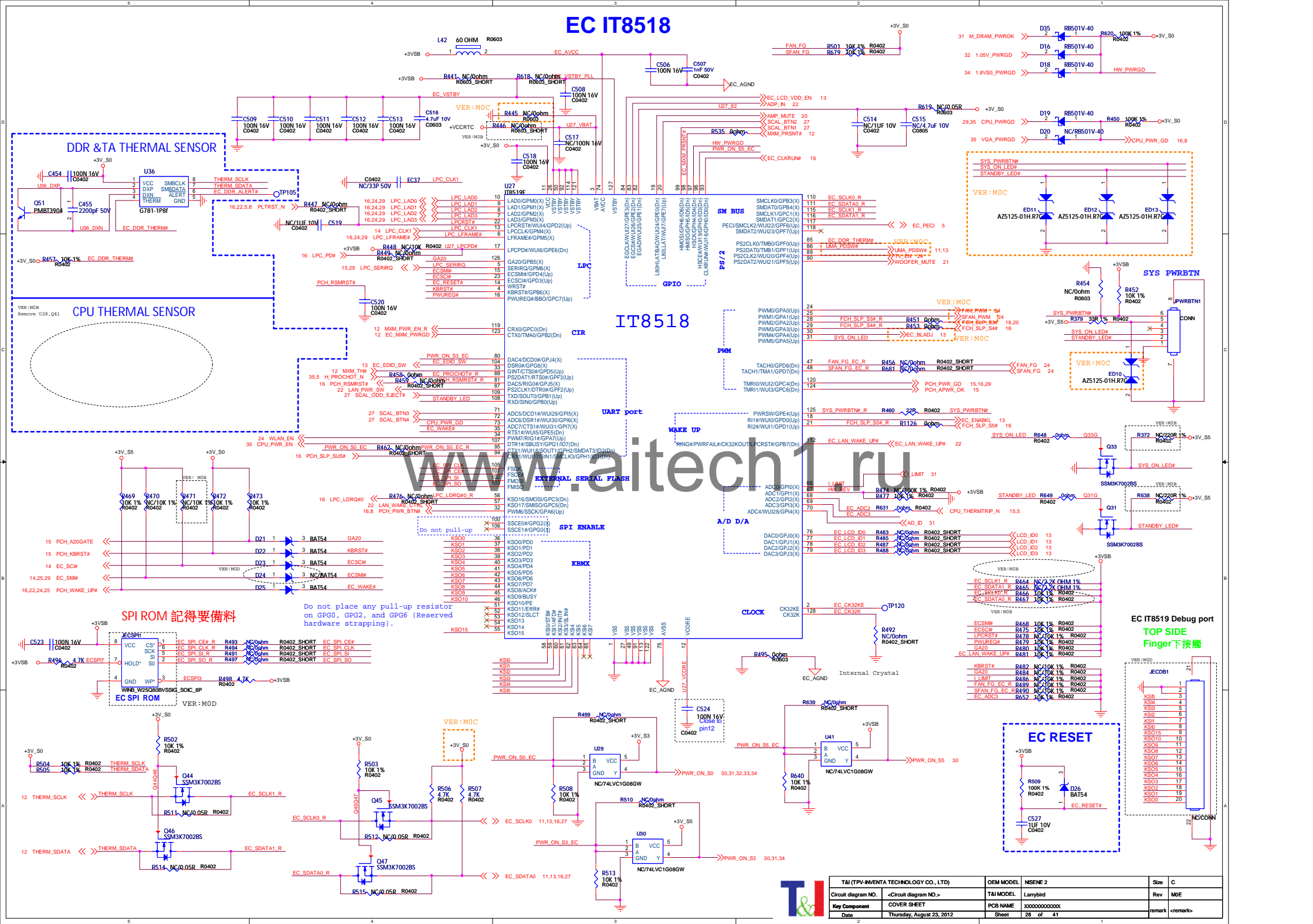


USB 2.0 (Dongle)



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
COVER SHEET		PCB NAME	X0000000000X	MOE
Key Component		Sheet	26 of 41	remark
Date	Thursday, August 23, 2012			<remark>

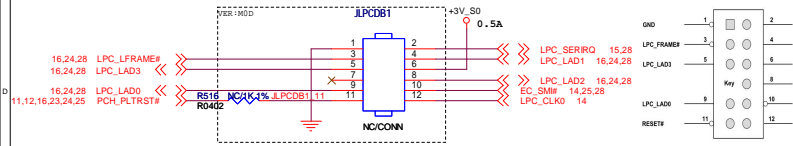
EC IT8518



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MDE
Key Component	COVER SHEET	PCB NAME	X00000000000X	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	28 of 41		

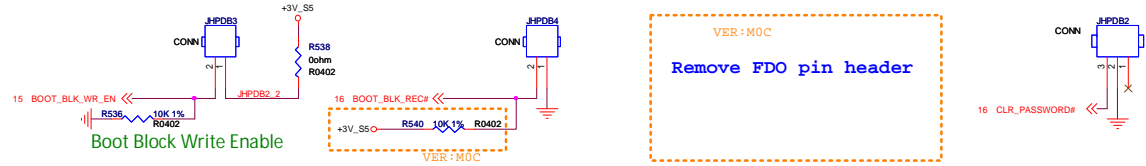
HP LPC DEBUG PIN HEADER

LPC Header

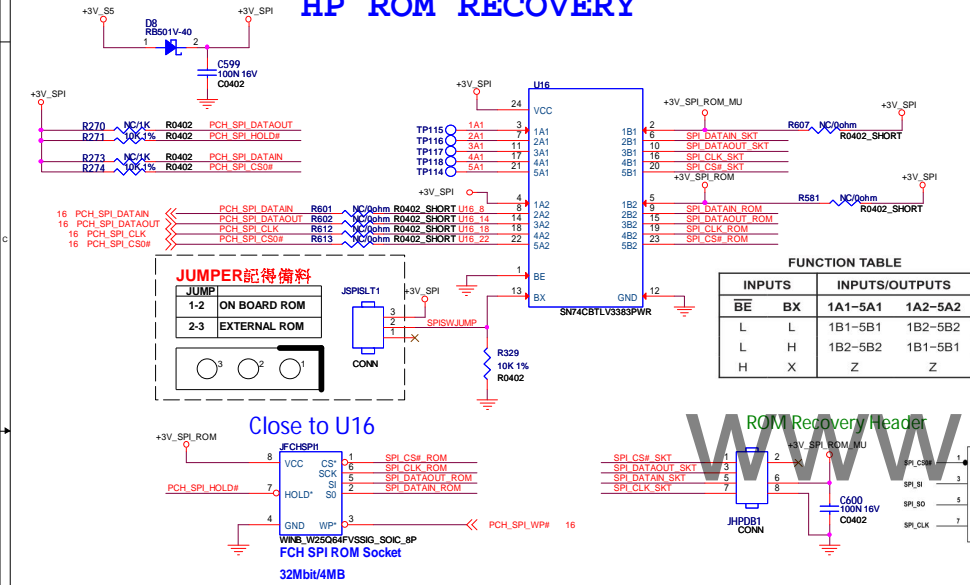


HP Header	Function
FDO	default: Low Jumper:High
CLR_PASSWORD#	default: high Jumper:low
BOOT_BLK_REC#	default:high Jumper:low

HP REQUEST PIN HEADER

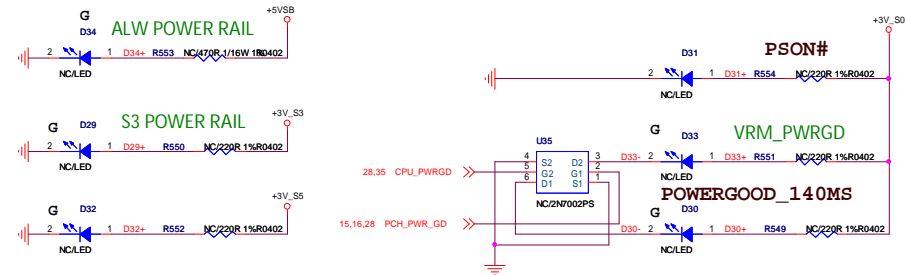


HP ROM RECOVERY



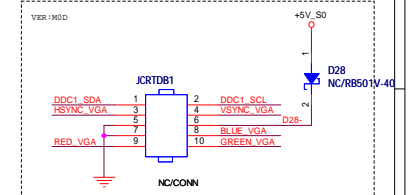
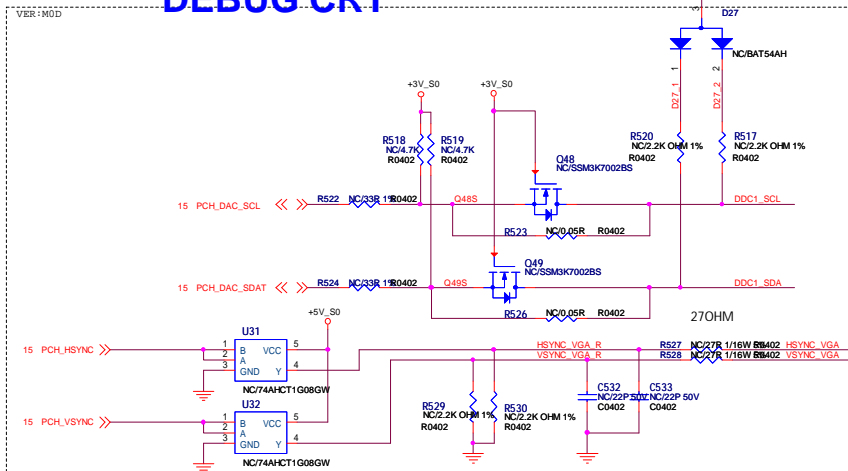
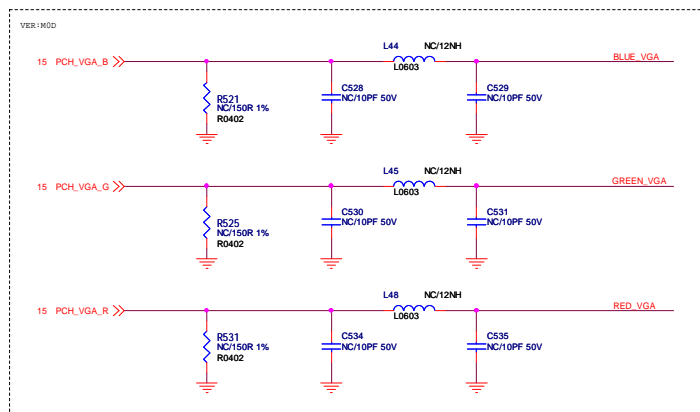
AUX_POWER

HP Indicator LED



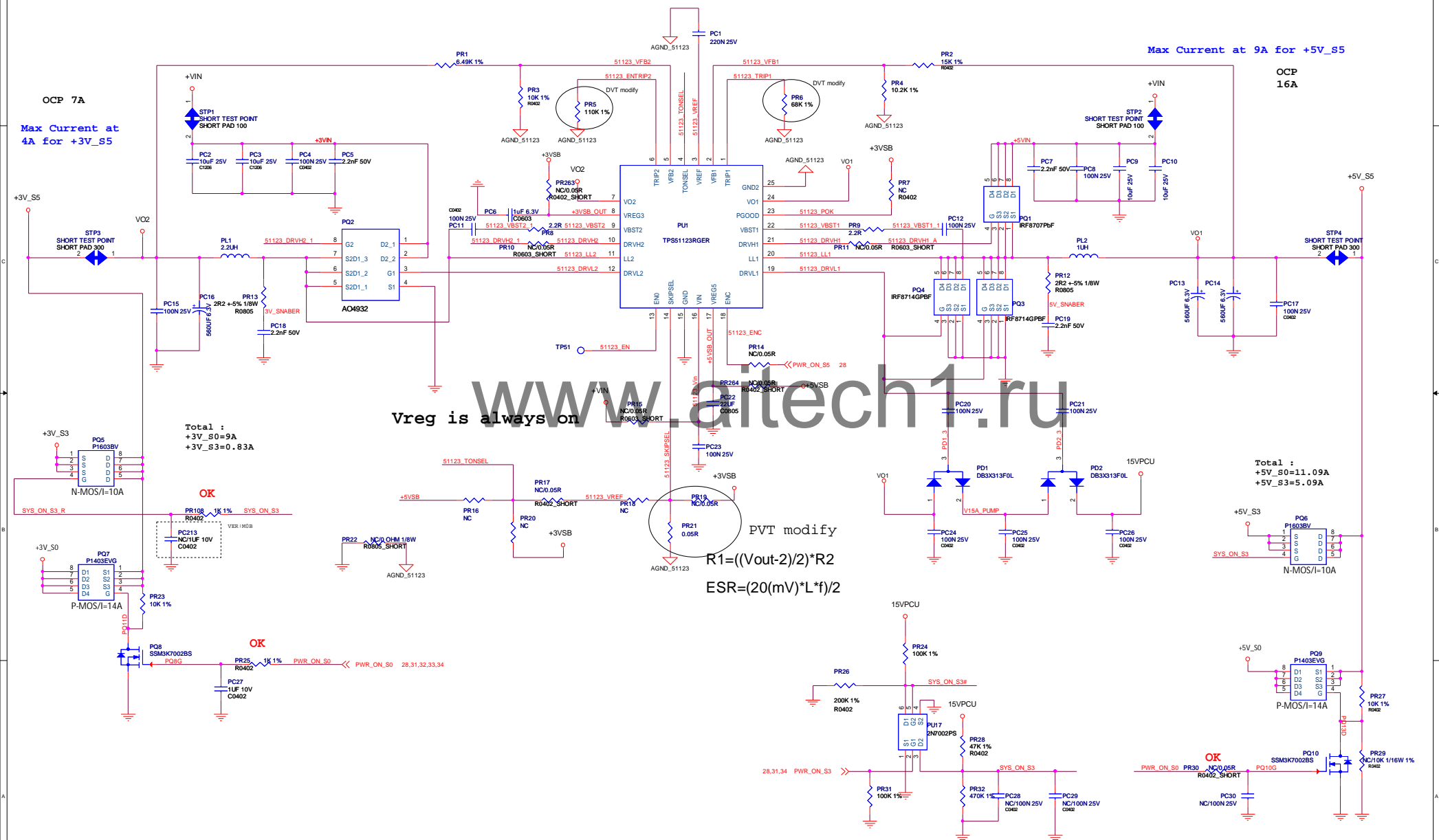
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DEBUG CRT



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXXX	MOE
Date	Thursday, August 23, 2012	Sheet	29 of 41	remark

**SYSTEM +3V_S5/+3V_S3/+3V_S0
+5V_S5/+5V_S3/+5V_S0**



+1.5V_SUS, MEM_VTT, DC-IN

TOTAL POWER	I_LIMIT
0W	0V
10W	0.1282V
20W	0.2564V
30W	0.3846V
40W	0.5128V
50W	0.6410V
60W	0.7692V
70W	0.8974V
80W	1.0256V
90W	1.1538V
100W	1.2820V
110W	1.4102V
120W	1.5384V
130W	1.6666V
140W	1.7948V
150W	1.9230V
160W	2.0512V
170W	2.1794V
180W	2.3076V
190W	2.4359V
200W	2.5641V
210W	2.6923V
220W	2.8205V
230W	2.9487V

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$$V_{out} = 0.704V * (R1 + R2) / R2$$

$$ESR = L * f / 70$$

MEM_VTT Power

Max Current at 7A for +1.5V_SUS

OCp 12A

Max Current at 1A for +MEM_VTT

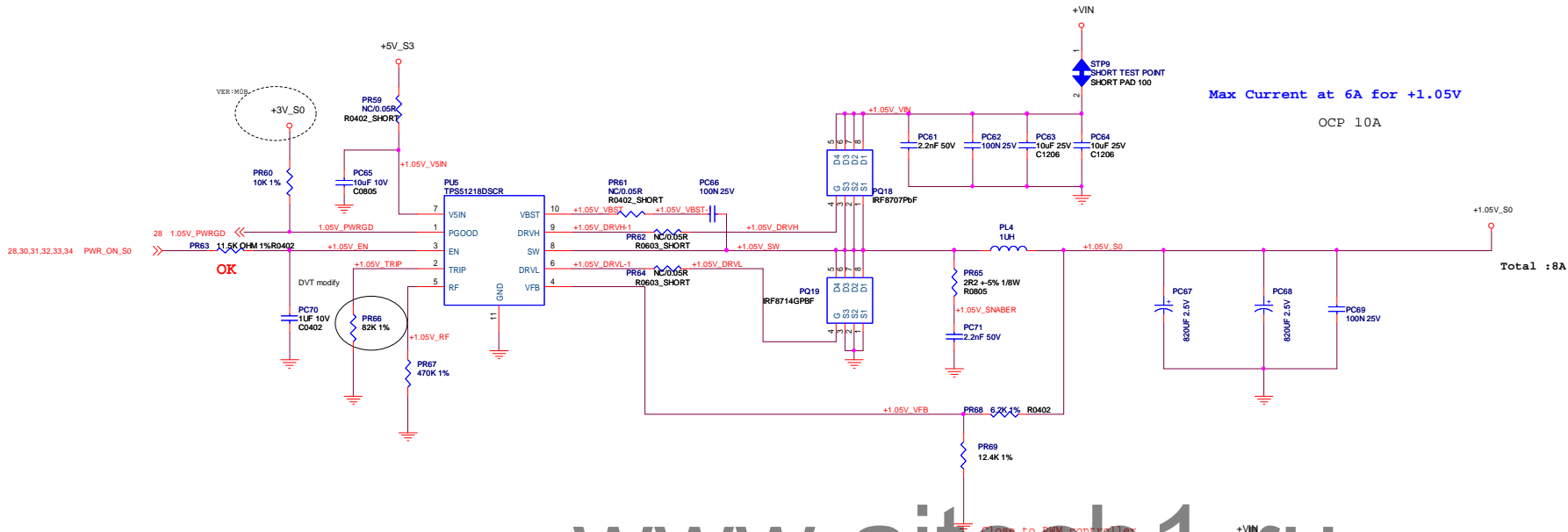
PVT modify

Adapter	AD_ID
120W	1.08V
150W	1.77V
180W	2.24V



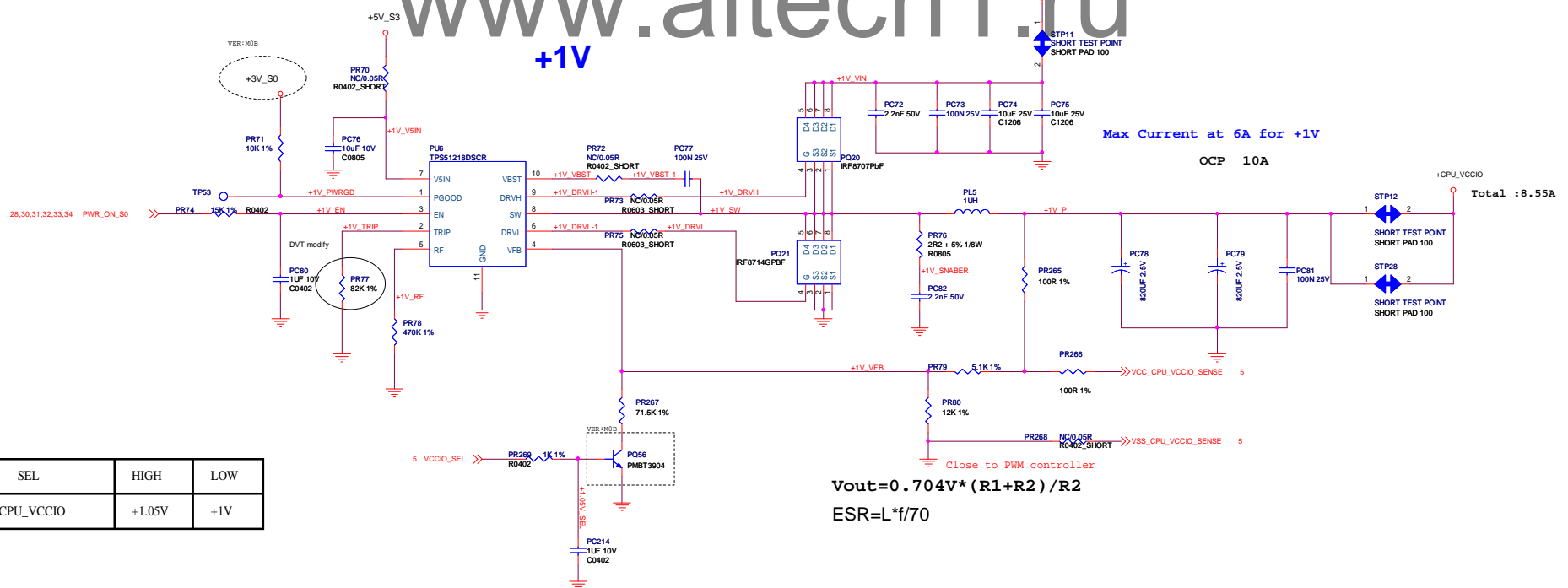
T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
COVER SHEET		PCB NAME	X0000000000X	MDE
Date	Thursday, August 23, 2012	Sheet	31 of 41	remark

+1.05V



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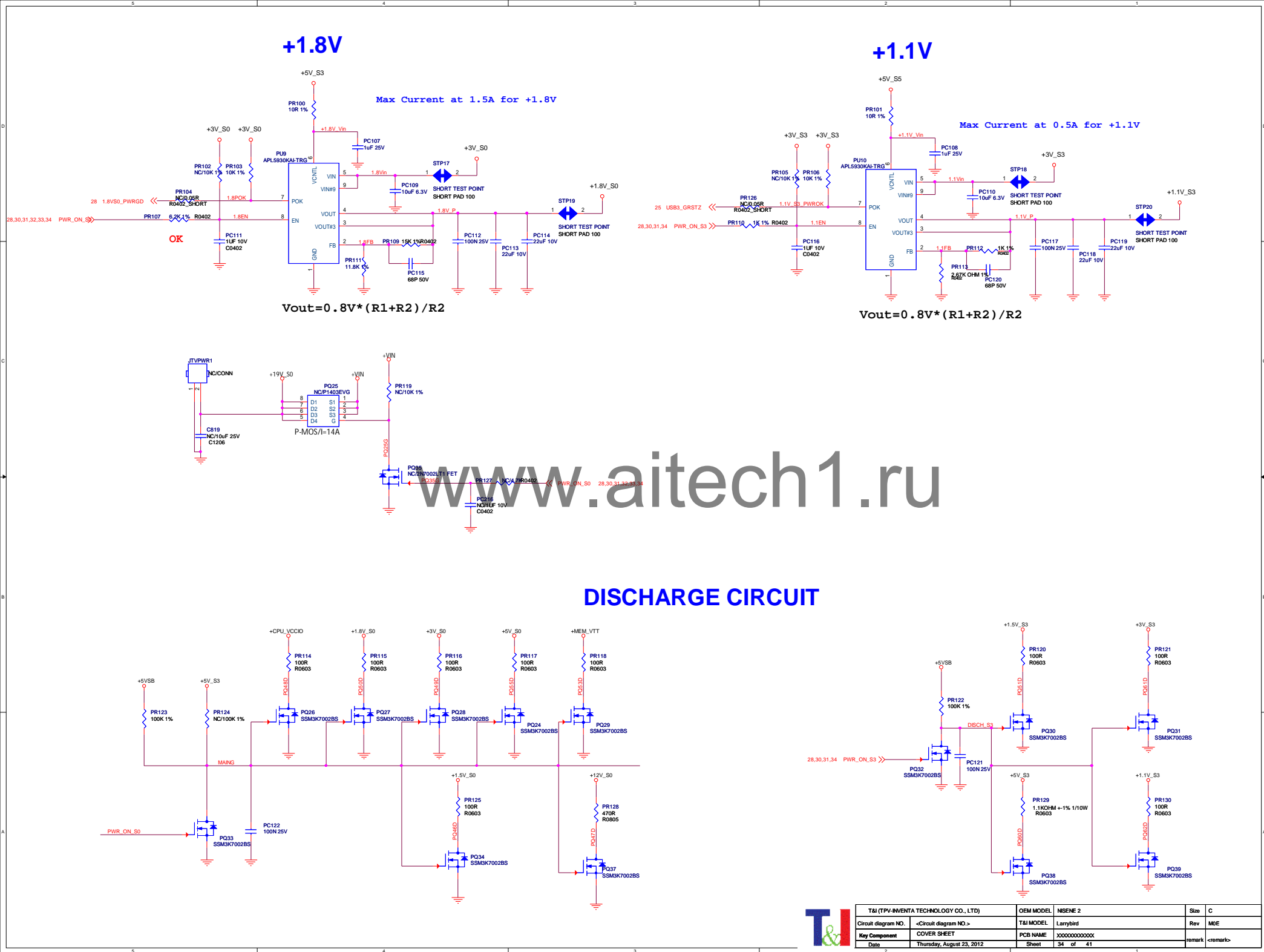
+1V



SEL	HIGH	LOW
+CPU_VCCIO	+1.05V	+1V



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)	OEM MODEL	NISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev
Key Component	COVER SHEET	PCB NAME	X000000000000	remark
Date	Thursday, August 23, 2012	Sheet	32 of 41	<remark>



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POWER SEQUENCE

Power ON

Power OFF

COIN BATTERY 3V

Net Name
RTC_BAT

RTC_RST

DC_IN

VIN = +19V

LDO OUT

+3VSB/+5VSB

POWER BTN to EC

SYS_PWRBTN#

PCH OUT TO EC (don't pull up)

PCH_SLP_SUS#

PCH OUT/IN

SUSWARN#&SUSACK#

EC OUT

PWR_ON_S5

POWER IC

+3V_S5/+5V_S5

EC OUT TO PCH

PCH_RSMRST#

EC OUT TO PCH

PCH_DPWR0K

EC TO PCH

PCH_PWR_BTN#

PCH TO EC

NC_SLP_S5_N

PCH TO EC

PCH_SLP_S4#

TP

PCH_SLP_LAN#>PCH_SLP_A#

PCH OUT

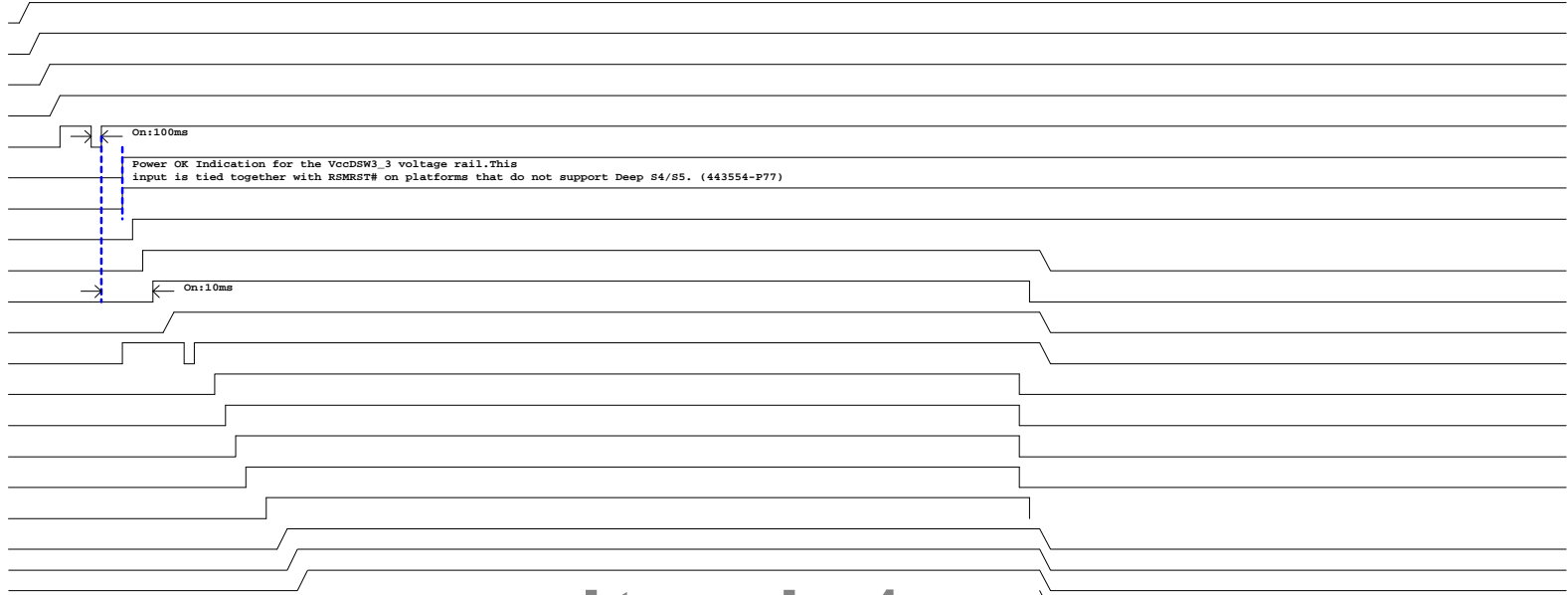
PCH_SLP_S3#

EC OUT

PWR_ON_S3

POWER IC
& MOS

+3v_S3
+5V_S3
+1.5V_S3



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S0 PWR

KBC OUT

PWR_ON_S0

FOR MXM
DESIGN

+5V_S0/+3V_S0

PCH ALL POWER

+MEM_VTT
+1.2V_S0
+1.8V_S0
+1.5V_S0
+1.1V_S0
+1.05V_S0
+0.85V_S0



LOGIC TO EC

HW_PWRGD

EC TO PCH(APWR0K)

PCH_APWR_OK

EC TO PCH

PCH_PWR_GD

EC TO VR PWR IC

CPU_PWR_EN

+CPU_VCC
+CPU_AXG

PWR TO KBC&PCH(SYS_PWR0K)

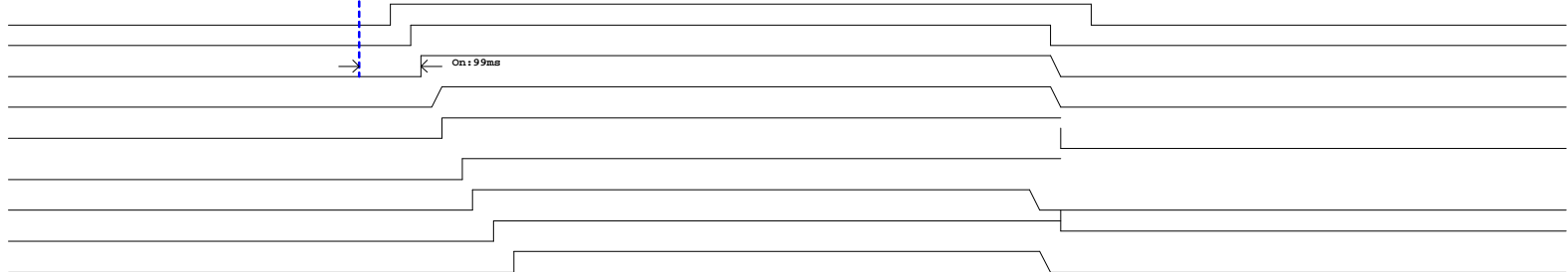
CPU_PWR_GD

PCH TO CPU

H_DRAMPWRGD

PCH TO CPU

H_PWRGD



PCH TO ALL

PLTRST_N



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	M0E
Key Component	COVER SHEET	PCB NAME	X0000000000X	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	37 of 41		

PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO0	AW55	I/O	3.3 V	Core	GPI	BMBUSY#	PU_PCH_BMBUSY
GPIO1	BR19	I/O	3.3 V	Core	GPI	TACH1	PU_PCH_GPIO1
GPIO2	BN9	I/OD	5 V	Core	GPI	PIRQE#	PIRQE_N
GPIO3	AV9	I/OD	5 V	Core	GPI	PIRQF#	PIRQF_N
GPIO4	BT15	I/OD	5 V	Core	GPI	PIRQG#	PIRQG_N
GPIO5	BR4	I/OD	5 V	Core	GPI	PIRQH#	PIRQH_N
GPIO6	BA22	I/O	3.3 V	Core	GPI	TACH2	PU_PCH_GPIO6
GPIO7	BR16	I/O	3.3 V	Core	GPI	TACH3	FDO
GPIO8	BP51	I/O	3.3 V	Suspend	GPO	NA	IGC_EN_N
GPIO9	BJ41	I/O	3.3 V	Suspend	Native	OC5#	USB_OC5#
GPIO10	BT45	I/O	3.3 V	Suspend	Native	OC6#	EC_SCI#
GPIO11	BN49	I/O	3.3 V	Suspend	Native	SMBALERT#	SMB_ALERT_N
GPIO12	BK50	I/O	3.3 V	Suspend	Native	LAN_PHY_PWR_CTRL	CLR_BIOS_DATA#
GPIO13	BA25	I/O	3.3 V	Suspend	GPI	HDA_DOCK_RST#	IO_PME_N
GPIO14	BM45	I/O	3.3 V	Suspend	Native	OC7#	EC_SMI#
GPIO15	BM55	I/O	3.3 V	Suspend	GPO	GPIO15	GPIO15
GPIO16	AU56	I/O	3.3 V	Core	GPI	SATA4GP	PCH_GPIO16
GPIO17	BT17	I/O	3.3 V	Core	GPI	TACH0	PCH_LEDID_SW
GPIO18	Mobile Only	I/O	3.3 V	Core	Native	NA	NA
GPIO19	AY52	I/O	3.3 V	Core	GPI	SATA1GP	SATA1GP
GPIO20	AV43	I/O	3.3 V	Core	Native	PCIECLKRQ2#	PCIE_LAN_CLKREQ#
GPIO21	BC54	I/O	3.3 V	Core	GPI	SATA0GP	SATA0GP
GPIO22	BA53	I/O	3.3 V	Core	GPI	SCLOCK	PCH_GPIO22
GPIO23	BA20	I/O	3.3 V	Core	Native	LDRQ1#	L_DRQ1_N
GPIO24	BP53	I/O	3.3 V	Suspend	GPO	MEM_LED	H_SKTOCC_N
GPIO25	Mobile Only	I/O	3.3 V	Suspend	Native	NA	NA
GPIO26	Mobile Only	I/O	3.3 V	Suspend	Native	NA	NA
GPIO27	BJ43	I/O	3.3 V	DSW	GPI	GPIO27	PU_PCH_GP27
GPIO28	BJ55	I/O	3.3 V	Suspend	GPO	GPIO28	SLP_LAN_N
GPIO29	BH49	I/O	3.3 V	Suspend	GPI	SLP_LAN#	PCIE_LAN_CLKREQ#
GPIO30	BU46	I/O	3.3 V	Suspend	Native	SUSWARN#	PCH_SUS_WARN#
GPIO31	BG43	I/O	3.3 V	DSW	GPI	GPIO31	PU_PCH_GP31
GPIO32	BC56	I/O	3.3 V	Core	GPO	CLKRUN#	EC_CLKRUN#



T&I (TPV-INVENTA TECHNOLOGY CO., LTD)		OEM MODEL	ISENE 2	Size	C
Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MDE
Key Component	COVER SHEET	PCB NAME	XXXXXXXXXXXXX	remark	<remark>
Date	Thursday, August 23, 2012	Sheet	38 of 41		

PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO33	BC25	I/O	3.3 V	Core	GPO	NA	SOP_ENABLE_GP33
GPIO34	BL56	I/O	3.3 V	Core	GPI	STP_PCI#	PU_PCH_GPIO34
GPIO35	BJ57	I/O	3.3 V	Core	GPO	NMI#	No connected
GPIO36	BB55	I/O	3.3 V	Core	GPI	SATA2GP	PCH_GPIO36
GPIO37	BG53	I/O	3.3 V	Core	GPI	SATA3GP	PCH_GPIO37
GPIO38	BE54	I/O	3.3 V	Core	GPI	SLOAD	BOARD_ID0
GPIO39	BF55	I/O	3.3 V	Core	GPI	SDATAOUT0	REV_ID0
GPIO40	BD41	I/O	3.3 V	Suspend	Native	OC1#	USB_OC1#
GPIO41	BG41	I/O	3.3 V	Suspend	Native	OC2#	USB_OC2#
GPIO42	BK43	I/O	3.3 V	Suspend	Native	OC3#	USB_OC3#
GPIO43	BP43	I/O	3.3 V	Suspend	Native	OC4#	USB_OC4#
GPIO44	BL54	I/O	3.3 V	Suspend	Native	PCIECLKRQ5#	PCIE_WLAN_CLKREQ#
GPIO45	AV44	I/O	3.3 V	Suspend	Native	PCIECLKRQ6#	PCIE_TV_CLKREQ#
GPIO46	BP55	I/O	3.3 V	Suspend	Native	PCIECLKRQ7#	PCIE_USB3_CLKREQ#
GPIO47	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO48	AW53	I/O	3.3 V	Core	GPI	SDATAOUT1	REV_ID1
GPIO49	BA56	I/O	3.3 V	Core	GPI	SATA5GP	BOARD_ID1
GPIO50	BT5	I/O	5.0 V	Core	Native	REQ1#	REQ1_N
GPIO51	AV8	I/O	3.3 V	Core	Native	GNT1#	GNT1-
GPIO52	BK8	I/O	5.0 V	Core	Native	REQ2#	REQ2_N
GPIO53	BU12	I/O	3.3 V	Core	Native	GNT2#	GNT2-
GPIO54	AV11	I/O	5.0 V	Core	Native	REQ3#	REQ3_N
GPIO55	BE2	I/O	3.3 V	Core	Native	GNT3#	GNT3-
GPIO56	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO57	BT53	I/O	3.3 V	Suspend	GPI	NA	CLR_PASSWORD#
GPIO58	BJ46	I/O	3.3 V	Suspend	Native	SML1CLK	EC_SCLK0
GPIO59	BM43	I/O	3.3 V	Suspend	Native	OC0#	USB_OC0#
GPIO60	BU49	I/O	3.3 V	Suspend	Native	SML0ALERT#	PCH_GP60_UP
GPIO61	BN54	I/O	3.3 V	Suspend	Native	SUS_STAT#	LPC_PD#
GPIO62	BA47	I/O	3.3 V	Suspend	Native	SUSCLK	BOOT_BLK_REC#
GPIO63	BH50	I/O	3.3 V	Suspend	Native	SLP_S5#	FCH_SLP_S5#
GPIO64	AT9	I/O	3.3 V	Core	Native	CLKOUTFLEX0	No connected
GPIO65	BA5	I/O	3.3 V	Core	Native	CLKOUTFLEX1	Test Point



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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MDE
Key Component	COVER SHEET	PCB NAME	X0000000000X	remark	<remark>
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PCH GPIO TABLE

PIN Name	Ball Name	Type	Tolerance	Power Well	Default	Multi Functional	Current Net Name
GPIO66	AW5	I/O	3.3 V	Core	Native	CLKOUTFLEX2	Test Point
GPIO67	BA2	I/O	3.3 V	Core	Native	CLKOUTFLEX3	Test Point
GPIO68	BU16	I/O	3.3 V	Core	GPI	TACH4	BOOT_BLK_WR_EN
GPIO69	BM18	I/O	3.3 V	Core	GPI	TACH5	PU_PCH_GPIO69
GPIO70	BN17	I/O	3.3 V	Core	Native	TACH6	PU_PCH_GPIO70
GPIO71	BP15	I/O	3.3 V	Core	Native	TACH7	SCAL_ODD_LED
GPIO72	AV46	I/O	3.3 V	Suspend	Native	BATLOW#	PCH_SPI_WP#_Q
GPIO73	Mobile Only	I/O	3.3 V	Suspend	Native	NA	
GPIO74	BR46	I/O	3.3 V	Suspend	Native	SML1ALERT# or PCHHOT#	PCH_GP74_UP
GPIO75	BK46	I/O	3.3 V	Suspend	Native	SML1DATA	PU_SML11DATA

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Circuit diagram NO.	<Circuit diagram NO.>	T&I MODEL	Larrybird	Rev	MDE
Key Component	COVER SHEET	PCB NAME	X0000000000X	remark	<remark>
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Schematic Modify History

MOA to MOB

Page-5 ,Add C933 C994,Power suggesstion
R687 is change PART ID
Add net "VCC_CPU_+0.85V_SENSE"

Page-9, JDDR1 is change to 10.1mm height
Page-10, JDDR1 is change to 6.0mm height
Page-11, L62,L63 are change PART ID by buyer suggestion
"JLVDSI" reference is change to "UMA_CN1"
"CONVERTER_DPC_TXP0/1" net name are change to "CONVERTER_DPD_TXP0/1"
"CONVERTER_DPC_TXN0/1" net name are change to "CONVERTER_DPD_TXN0/1"
"CONVERTER_DPC_AUXP/N" net name are change to "CONVERTER_DPC_AUXP/N"

Page-12, C810~C817 are not stuff,R798,R799 are not stuff
Net "CPU_GFX_TXP0~15","CPU_GFX_TXN0~15","CPU_GFX_RXP0~15" and "CPU_GFX_RXN0~15"
serialc CAP are change to 0.22uF
Stuff R802,un-stuff R805 for Nvidia suggestion

Page-13,R838 is stuff,R1143 un-stuff for EC & BIOS suggestion
Add R1144,C991 for power soft star
Add net "EC_SCLK0","EC_SDATA0" for EDID flash issue

Page-14,Net "PCIE_TV_RXN/P" and "PCIE_TV_TXN/P" are change connect to PCH PCIE port5
Net "PCIE_WLAN_RXN/P" and "PCIE_WLAN_TXN/P" are change connect to PCH PCIE port6
Net "USB_OC6#" rename to EC_SCI# for BIOS suggestion

Page-15,R935 is change to 1K ohm,R331 is change to 0 ohm,R936 is change to 4.7k ohm follow Intel CRB
R951 and R952 are stuff 10k ohm to disable DDPB,DDPC
Net "PCH_DVI_DATA0~2P/N" are change to DDPC,Net "CONVERTER_DPDTX0~1P/N" are change to DDPD
ODD change to connect Net "SATA_RX4N/P" and "SATA_TX4N/P"
R940 and R941 are stuff 10k ohm,R946 and R947 are stuff 10k ohm

Page-16,X5 is changed PART ID by buyer suggestion
R1123 and R1020 are un-stuff,add R1121 for PCH clear CMOS
Add JME1 for BIOS request,add R1122 follow Intel CRB

Page-17,L59 is changed PART ID by buyer suggestion
Page-18,R1069 and R1070 are un-stuff for BIOS & EC suggestion
Page-19,R934 is un-stuff for can't boot issue
Page-20,JMIC1 is change PART ID by buyer suggestion
Page-21,JHP1 and JLINEOUT1 change PART ID by buyer suggestion
Page-22,Remove Q50 for can't boot issue
Add 0ohm R1127,R373 is change to 2.2k ohm,Q32 is unstuff
Page-22,Remove Q50 for can't boot issue
Add 0ohm R1127,R373 is change to 2.2k ohm,Q32 is unstuff for 100mW issue

Page-23,JCR1 is change PART ID
JSATAHDD1 is change white color,JSATAODD1 is change blue color

Page-24,R384,R386,R392,R385,R389,R395,R579,R580 and R571 are change to 0805 footprint
Add 0ohm R621 reset signal for 80 port

Page-25,C921 and C922 are change 18pF for SI pass

Page-26,JUSB30L1,JUSB30L2,JUSBR0~3 and JUSBDON1 are change PART ID for ME height request

Page-27,Add R1141,R1142 for S3 wake
Add manual parts PCB1,CPU_BACK1,CPU_STAIN1,CPU HOLDER1,JECSPI2,JFCHSPI2,JUMPI~3 and JRTCBATT2

Page-28,U36 is change G781-1P8f,remove U28,Q41 for address conflick issue
R471 is un-stuff; R506,R507 are change connect to +3V_S5
R466,R467 are change to 10k ohm for <100mW issue

Page-29,Remove R332,R333,R334,R338,R342,R575,R576 and R577
Page-30,PR5,PR6 are change PART ID for power suggestion
PR19 is stuff,PR21 is un-stuff for AUDIO headphone in S3 noisy issue
Reserve PC213 for power suggestion

Page-31,PR41 is change PART ID for power suggestion
PC46, PR49, PU3, PR48 and PC47 are un-stuff for < 100mW issue

Page-32,PR60 and PR71 are change connect to +3V_S0
PR66 and PR77 are change PART ID for power suggestion
PQ56 is change use BJT for vlotage select issue

Page-33,PR82 is change connect to +3V_S0 ; PR88 PART ID is change,Add PR274 for CPU voltage sense
PQ58 is change use BJT for vlotage select issue

Page-35,PR134 is un-stuff for power sequence issue

Page-36,PR260 is change PART ID for power suggestion

MOB to M0C

Page-1 Change H4 H15 screw hole footprint for ME request.
Page-9,10 Pop C681 C704 cap value(2.2uF/0402) for 0.75V overshoot problem.
Page-11,28 Modify U43,pin10 (PD#) control method, DVT HW circuit control PVT EC(UMA_PDSW#) control.

Page-13,28 Modify backlight and LVDS 5V control method, DVT HW circuit control PVT EC(UMA_PDSW#) control.

Page-15 Non-pop R926 for BOOT_BLK_WR_EN function
Page-15,29 Remove FDO function, FDO function pin header combine with ME pin header, Add R925 remove JHPDB5, R537, R539

Page-16 Pop R988, for clear password function.
Page-16 Non-pop R1005 R1006(0ohm), for leakage problem.
Page-16 PVT JME1 change name to JFDO.

Page-22 D15 PVT change to white LED.
Page-22 D12 D13 change to EVT LED parts.
Page-22 Modify RJ45 circuit for ESD issue, Add R403 R416 R419 R423(0603/0ohm), add EU33 EU34 ED2

Page-22 Change RJ45 connector, for RJ45 LED color request.
Page-23 Change JSATAHDD1 and JSATAODD1 connector, for connector pin length too short problem.
Page-25 Add C403 C434, follow USB3.0 vendor suggest.
Page-28 Non-pop R445, for TnI EE design.
Page-28 Modify R506 R507 pull high voltage from 3V_S5 change to 3V_S0, for leakage problem.
Page-11,13,28 Modify U27,pin86(UMA_PDSW#) to control U43,pin10 (PD#) ,backlight enable and LVDS 5V enable.

Page-13,24,28 Swap U27 pin25 and pin30, for meet panel converter board pwm frequence request.
Page-29 Add R540(10Kohm) pull high to 3V_S5, for BOOT_BLK_REC# function.

Page-30 Non-pop PR19 Pop PR21, change power mode, from OOA mode change to skip mode.
Page-31 Remove PR54, PR54 change to default short footprint.
Page-12 Change MXM socket P/N.

Page-12 Change MXM_PRSNT# pull high source from +3V_S0 to +3VSB.

Page-20,21 Audio circuit supply power change to +3V_S3 +5V_S3 plane.

Page-9,10 Change DDR3 socket P/N 10.1mm and 6mm.

Page-27 Add CPU thermal hole myalr .

Page-22 (1) R343,R345,R346,R348,R349,R350 change footprint -> R0402_SHORT, for vendor suggest.
(2) De-pop R351,R353,R562,R635 for vendor suggest.
(3) Replace R365 to RJ45 pin13, and change value from 249ohm to 510ohm for vendor suggest.

Page-27 (1) Add 16pcs optical point.
(2) Reserve ED7 ED8 to touch screen USB signal.

Page-21 (1) Add C576 C577 for pop noise issue.
(2) Reserve C588 C590 for pop noise issue.

Page-28 Add ED10 ED11 ED12 ED13 (6011B0131701) for ESD 15KV request.

Page-22 (1) Modify RJ45 circuit for ESD issue, Add R380 0ohm (60130B00002T)
(2) R373 Change to 1Kohm

M0C to M0D

Page-8 JXDPCPU1 is un-stuff without debug port
Page-10 JDDR2 vendor is change to Tyco
Page-14 R876 is un-stuff for USB3.0 S3 wake issue
Page-27 JECSPI2,JFCHSPI2 are manual parts that change to SMT
Page-28 JECSP11 is change to not use ROM socket
D24 is un-stuff for USB3.0 S3 wake issue
JECDB1 is un-stuff with debug port for MP version
R379 is change to 33 ohm for HP power button LED brightness request

Page-29 JFCHSPI1 is change to not use ROM socket
D29~D34,R550~R554,R549,U35,L44,L45,L48,R521,R525,R531,C528~C535, ,U31,U32,R522,R524,R518 ,R519,Q48,Q49,D27,R520,R517,R527,R528,JCRTDB1 are un-stuff for MP version

M0D to M0E

Remove CPU frame line to avoid SMT issue

Page-21 JLINEOUT1 modify 2 pin footprint 1.35mm to 1.2mm for manufacturer issue

Page-22 Modify ED2 footprint to polarity marked



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